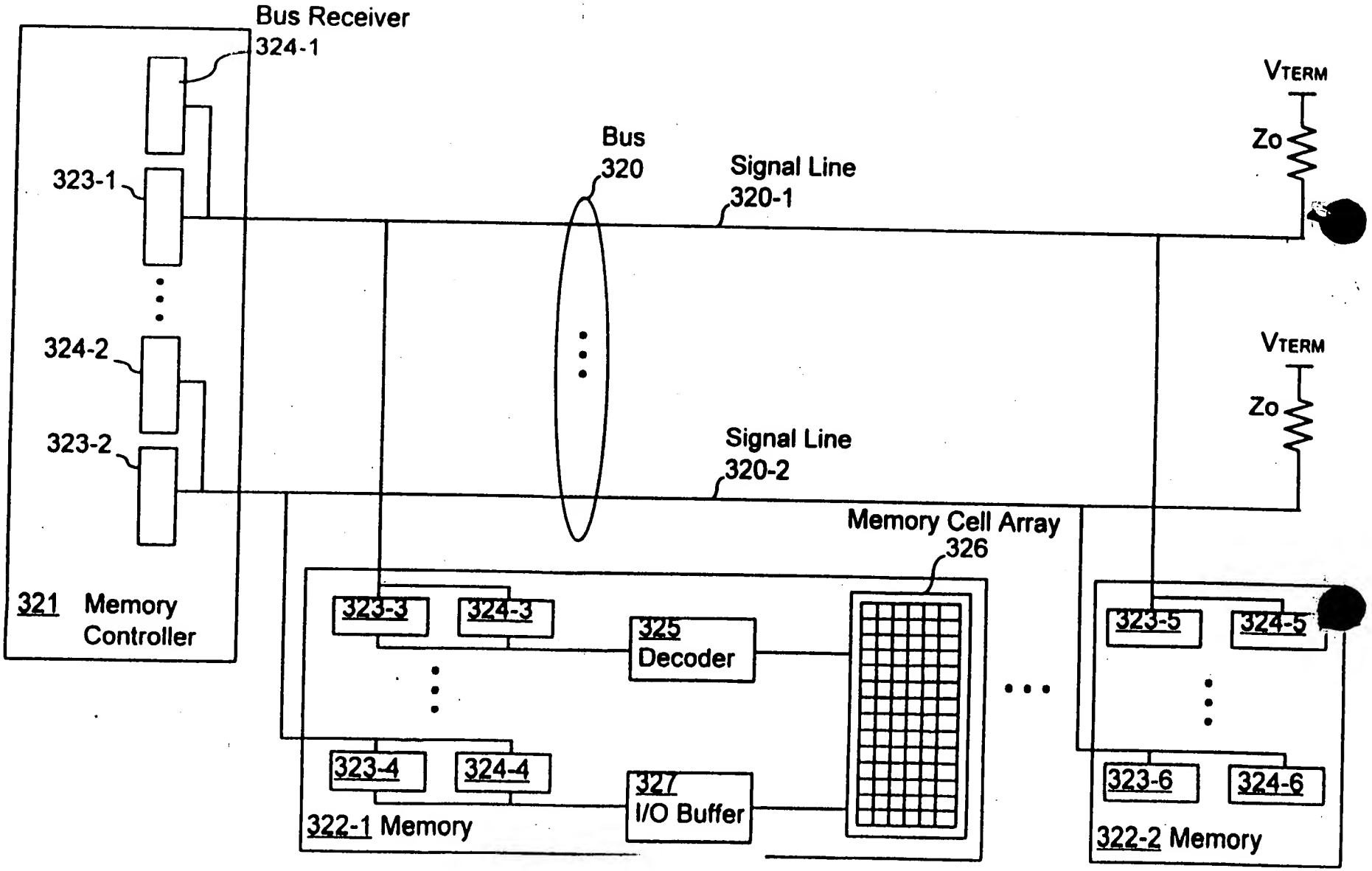

Bus Receiver
324-1
323-1
324-2
323-2
321 Memory Controller
Bus
320
Signal Line
320-1
Signal Line
320-2
VTERM
Zo
VTERM
Zo
Memory Cell Array
326
323-3
324-3
325
Decoder
323-4
324-4
327
I/O Buffer
322-1 Memory
323-5
324-5
323-6
324-6
322-2 Memory

FIG. 1

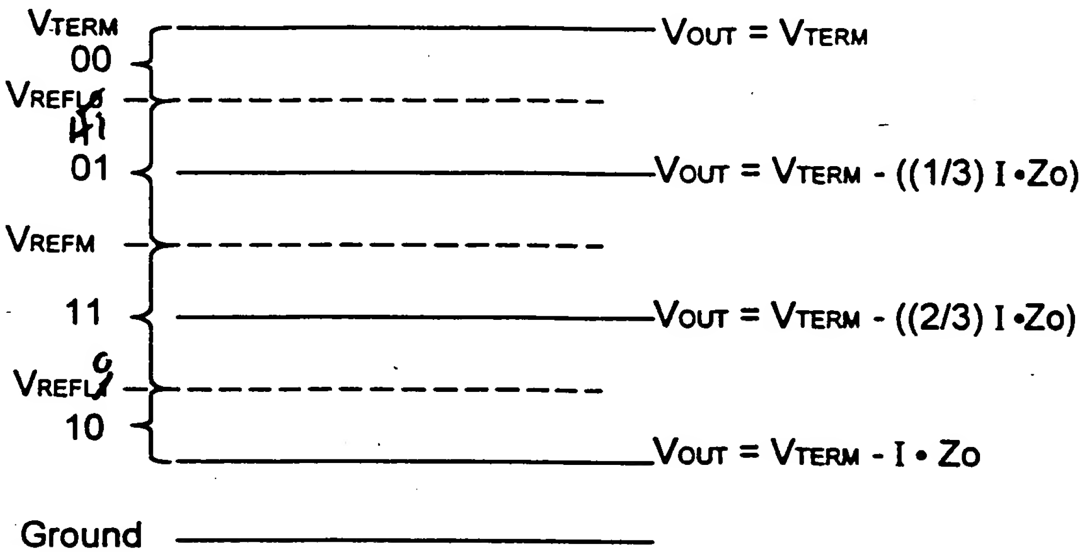


FIG. 2

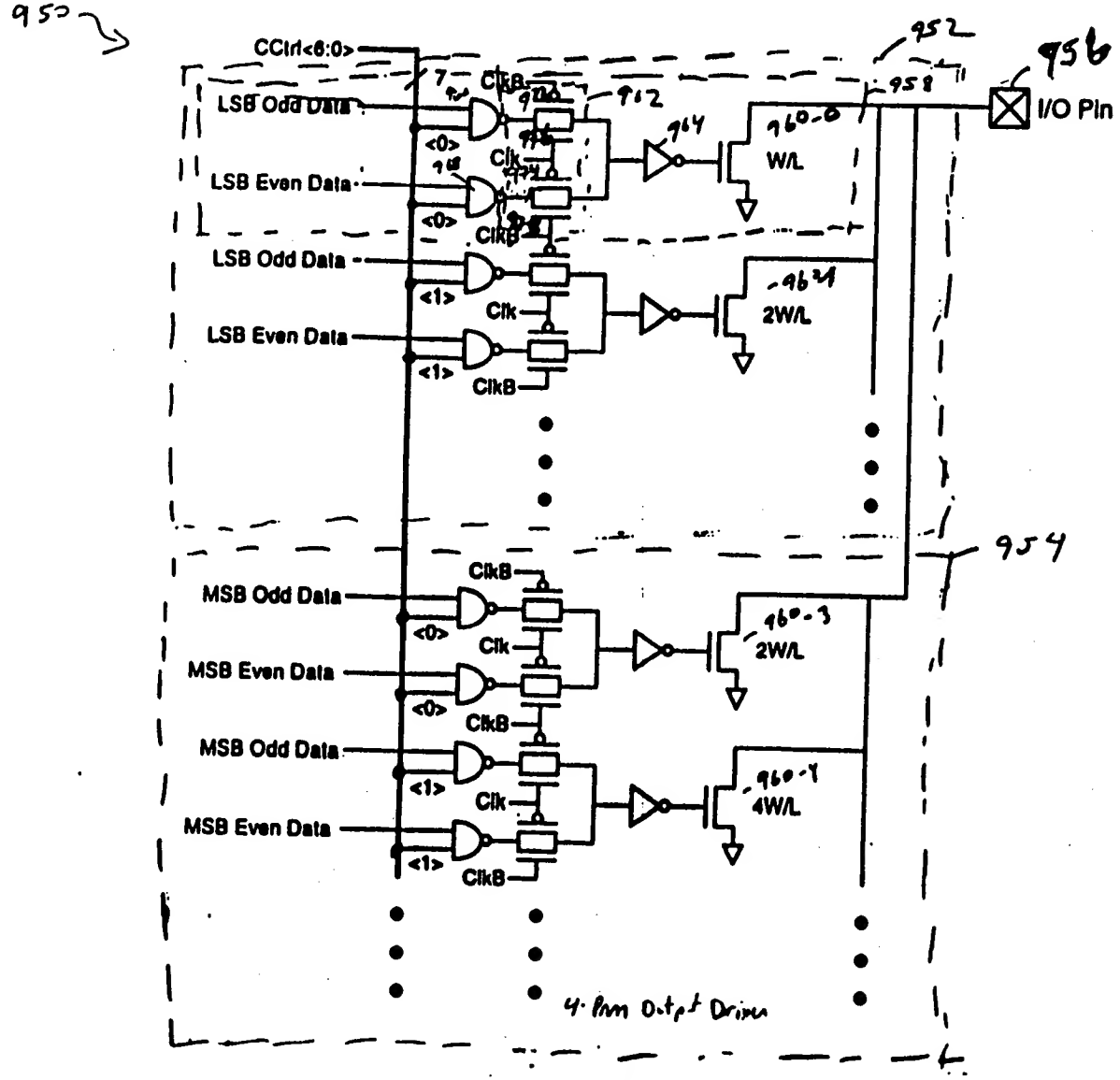

950
952
956
958
CCtrl<6:0>
I/O Pin
LSB Odd Data
LSB Even Data
MSB Odd Data
MSB Even Data
<0>
<1>
Clk
ClkB
W/L
2W/L
4W/L
954
4-Pin Output Driver

FIG. 3A

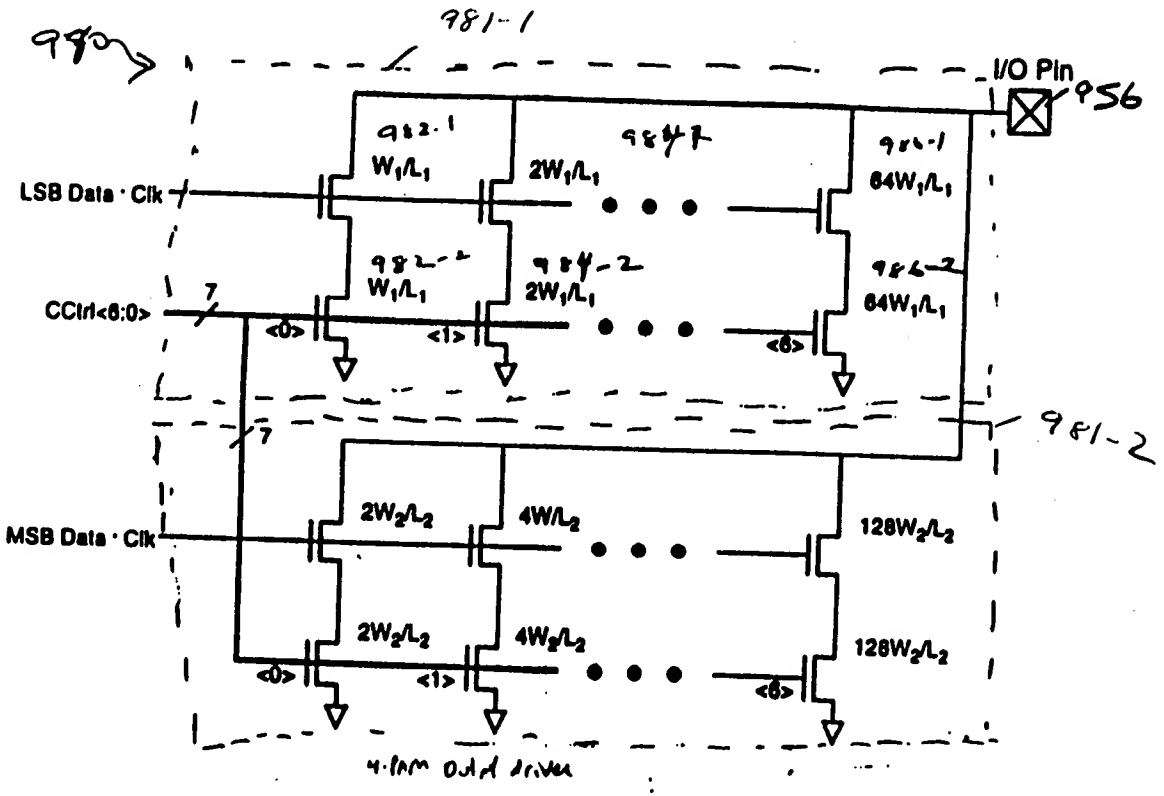

950
981-1
I/O Pin
956
LSB Data · Clk
CCtrl<6:0>
7
<0>
<1>
<6>
W_1/L_1
$2W_1/L_1$
$64W_1/L_1$
981-2
MSB Data · Clk
$2W_2/L_2$
$4W_2/L_2$
$128W_2/L_2$
4-bit odd driver

FIG 3B

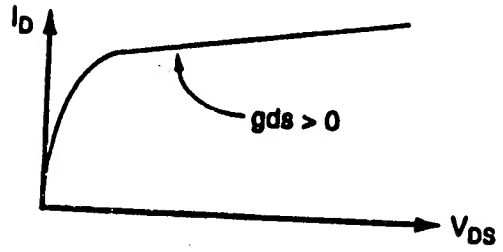


FIG 4A

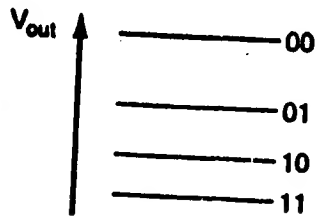


FIG. 4B

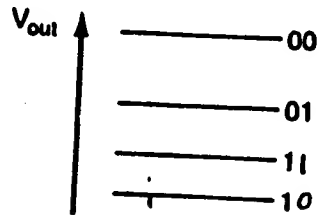
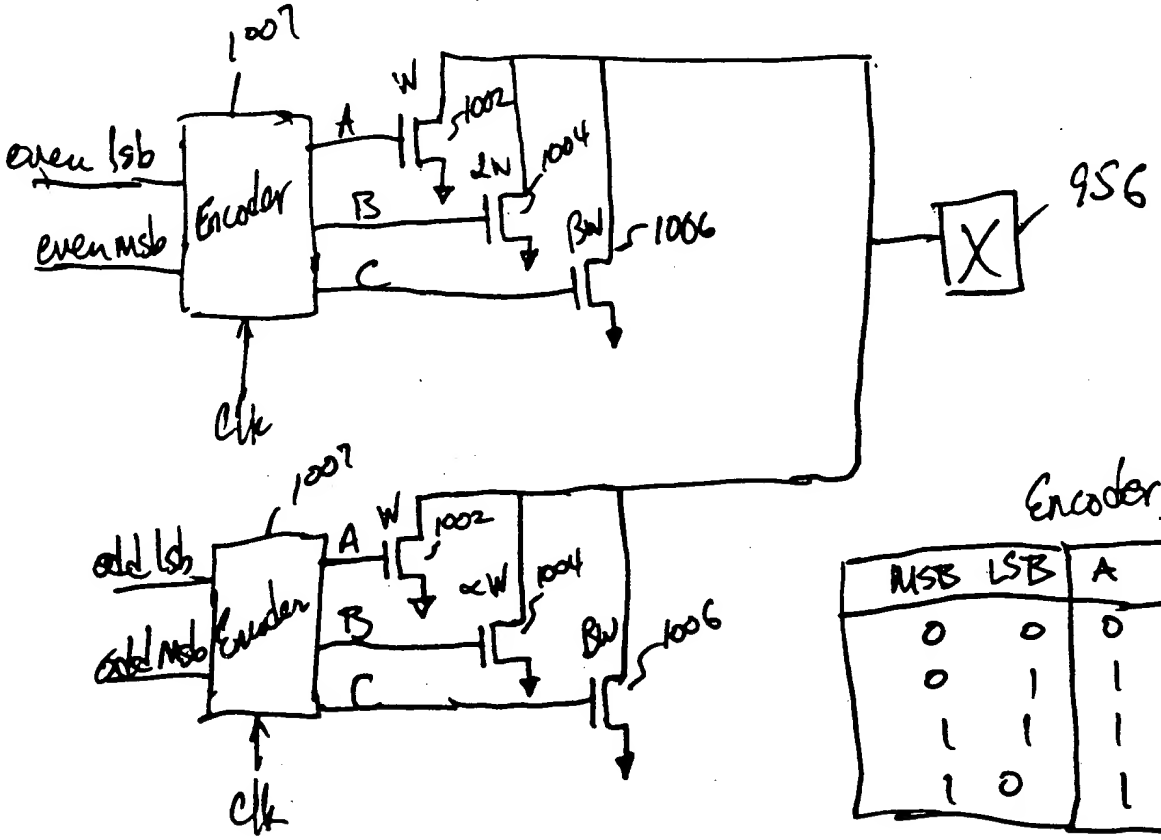


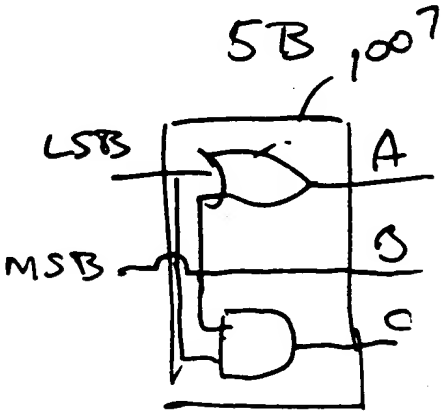
FIG. 4C

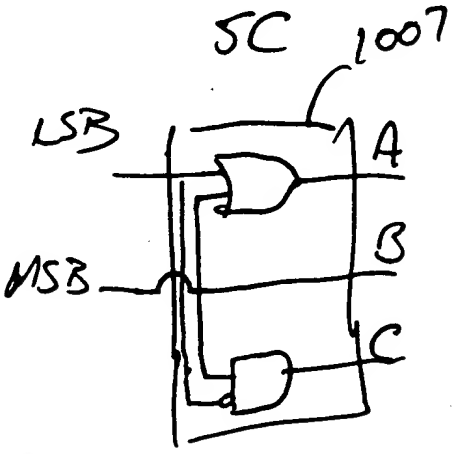
FIG. 5A

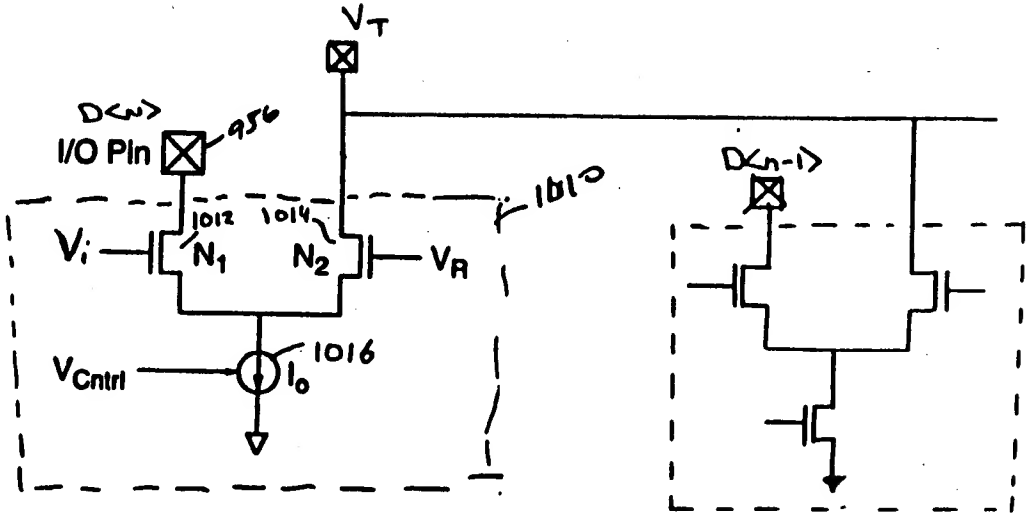


Encoder logic

MSB	LSB	A	B	C
0	0	0	0	0
0	1	1	0	0
1	1	1	1	0
1	0	1	1	1







circuit to Reduce Switching Noise

FIG 6

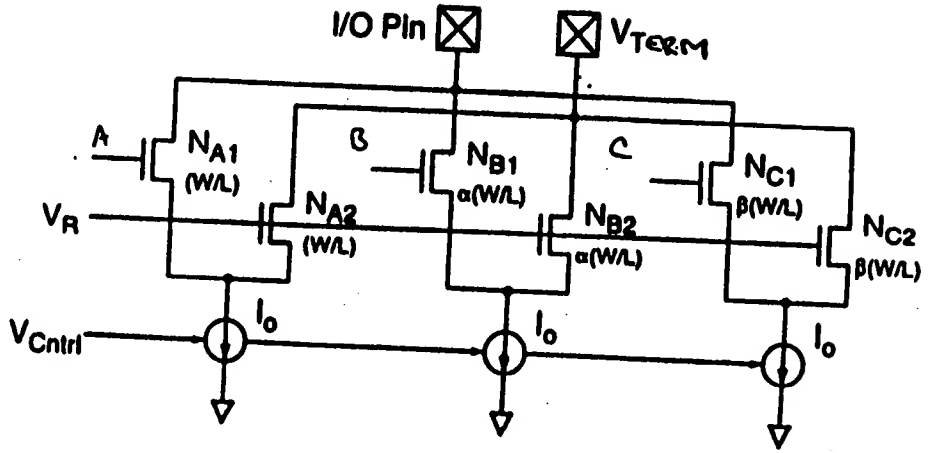
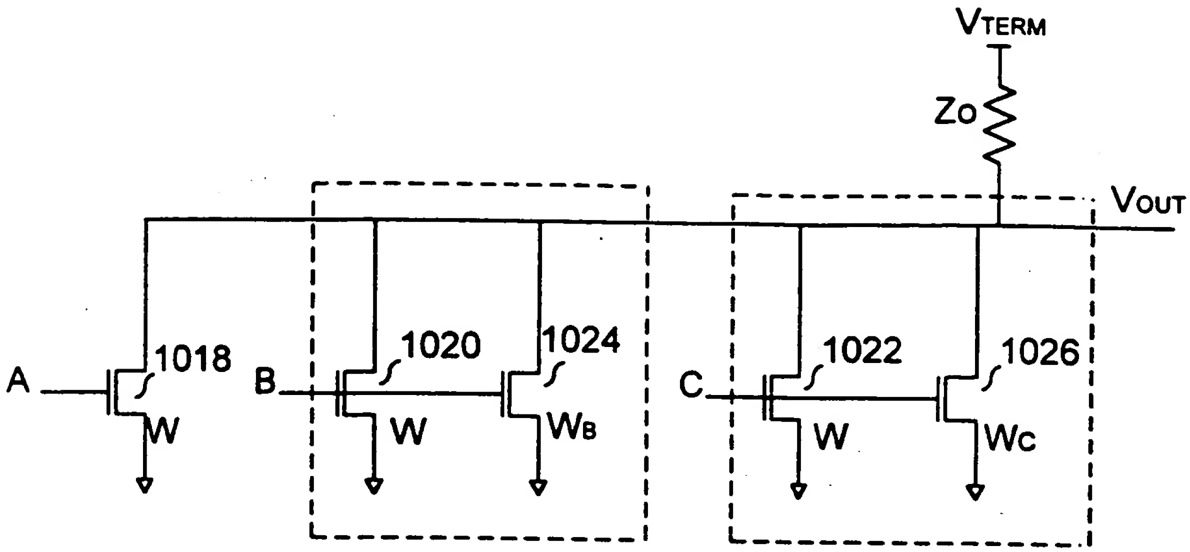
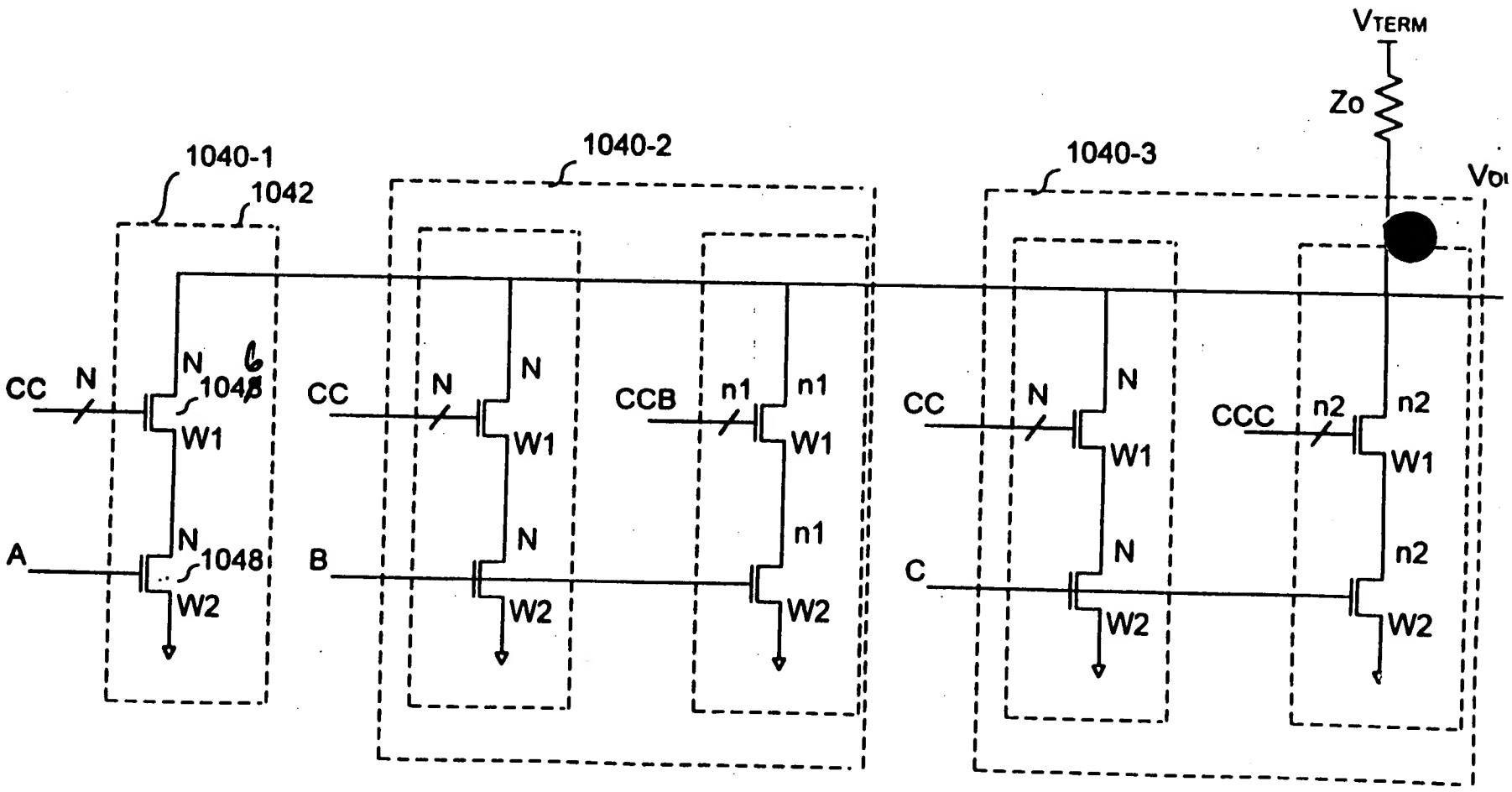


FIG. 7



GDS Compensated Multi-PAM Output Driver

FIG. 8



GDS Compensated Multi-PAM Output Driver with Current Control

FIG. 9A

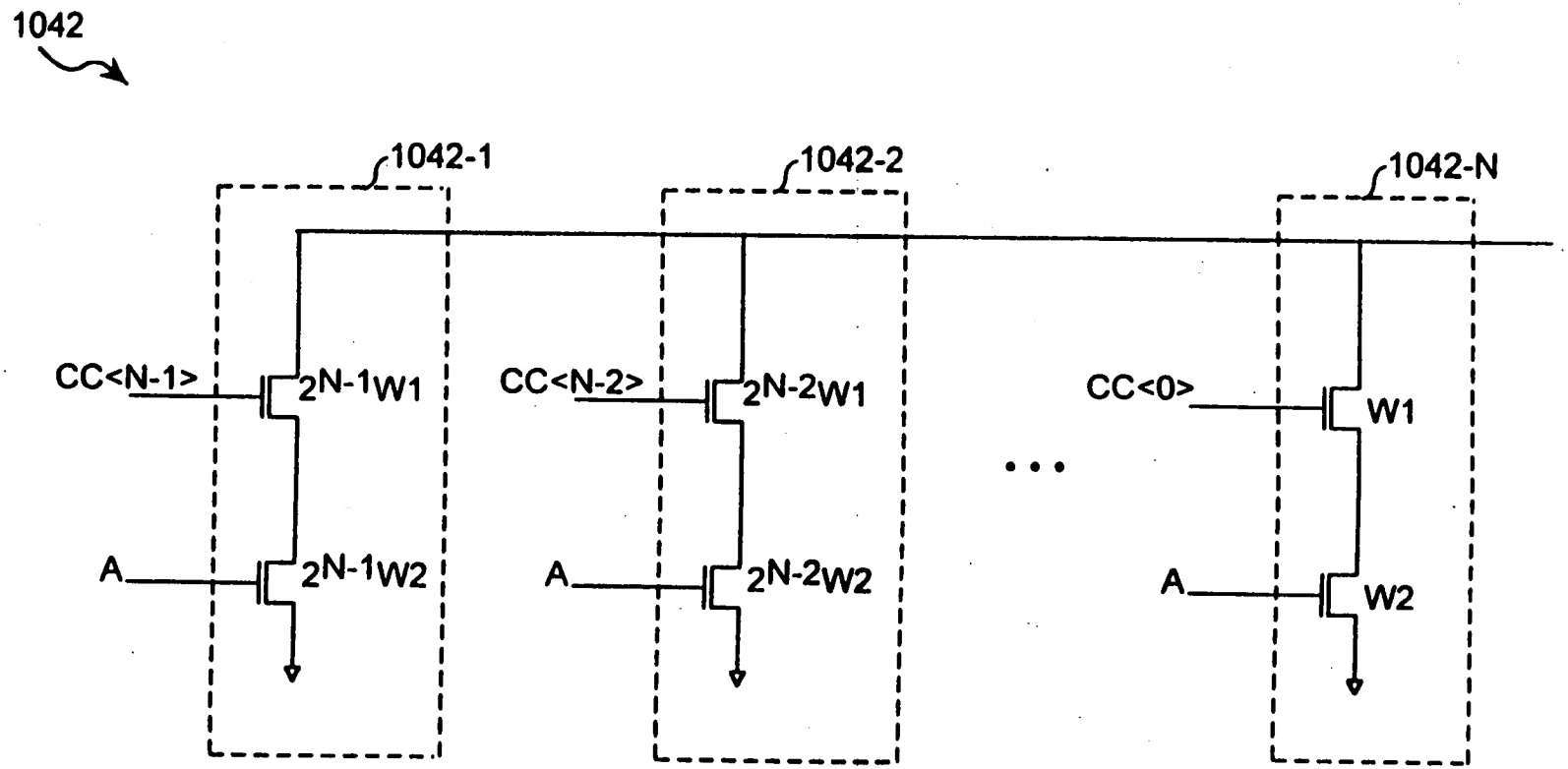


FIG. 9B

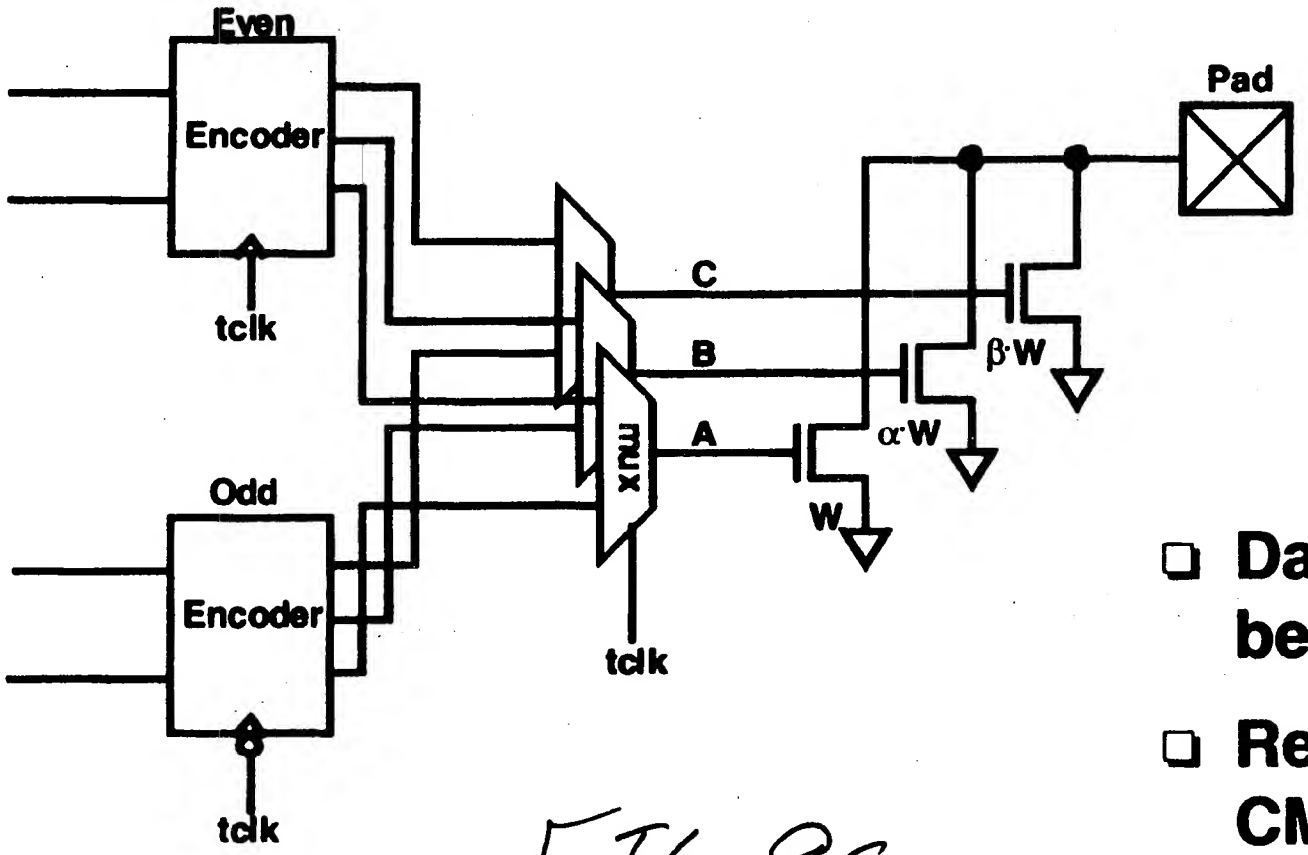
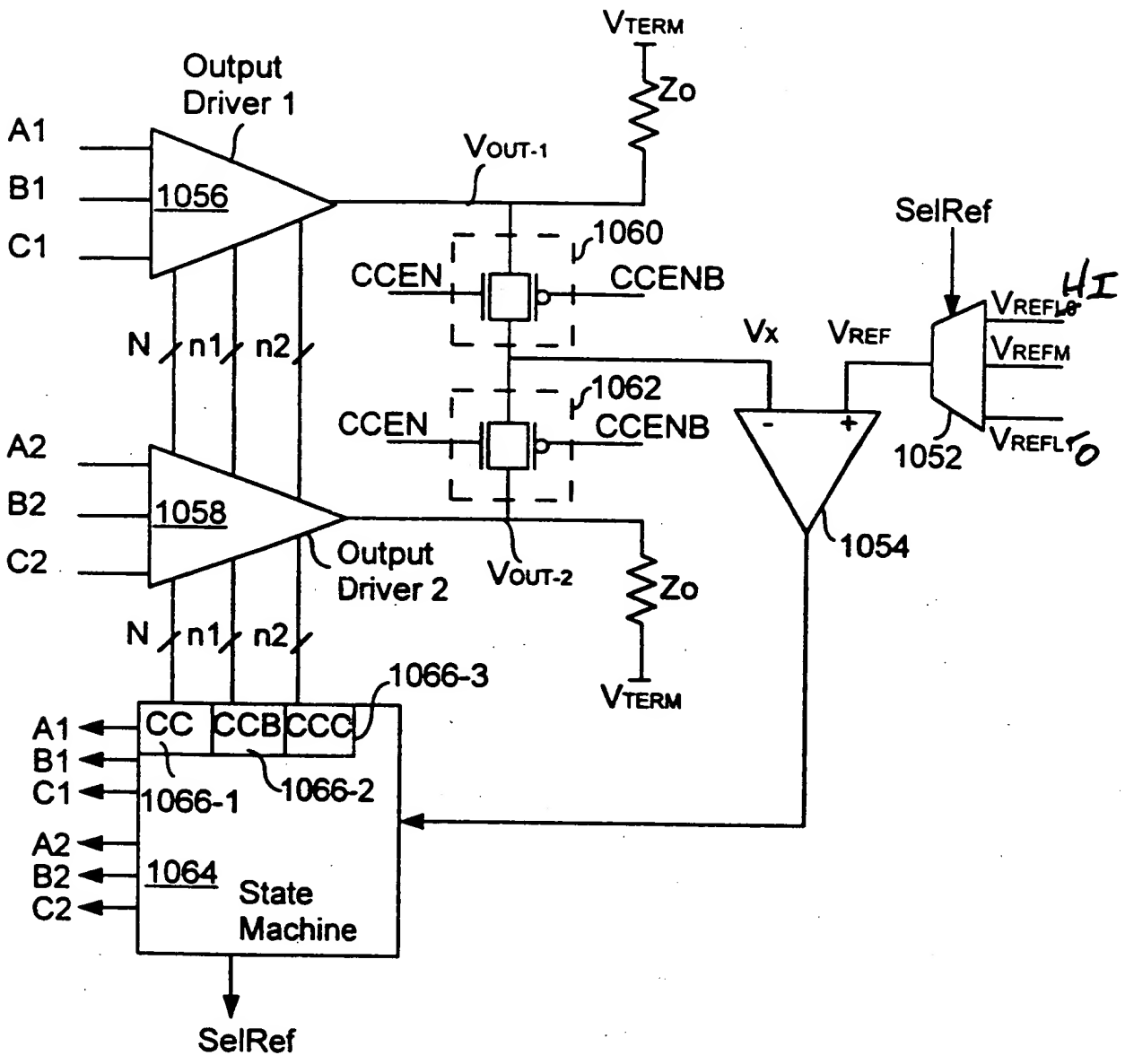


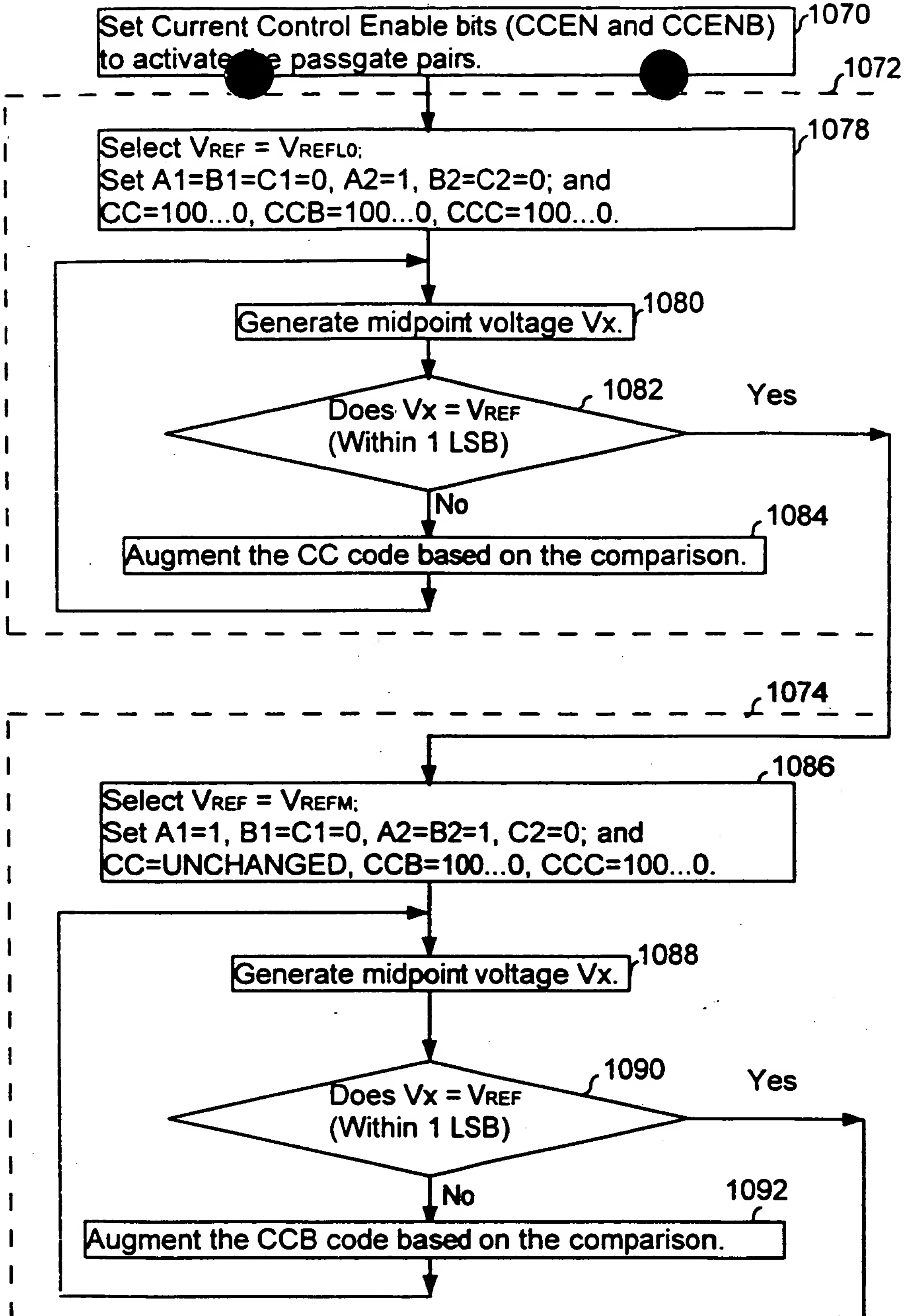
FIG. 9C

- Data muxed before pad
- Requires running CMOS signals A,B,C @ full frequency



Circuit for Calibrating the GDS Compensated Output Driver with Current Control

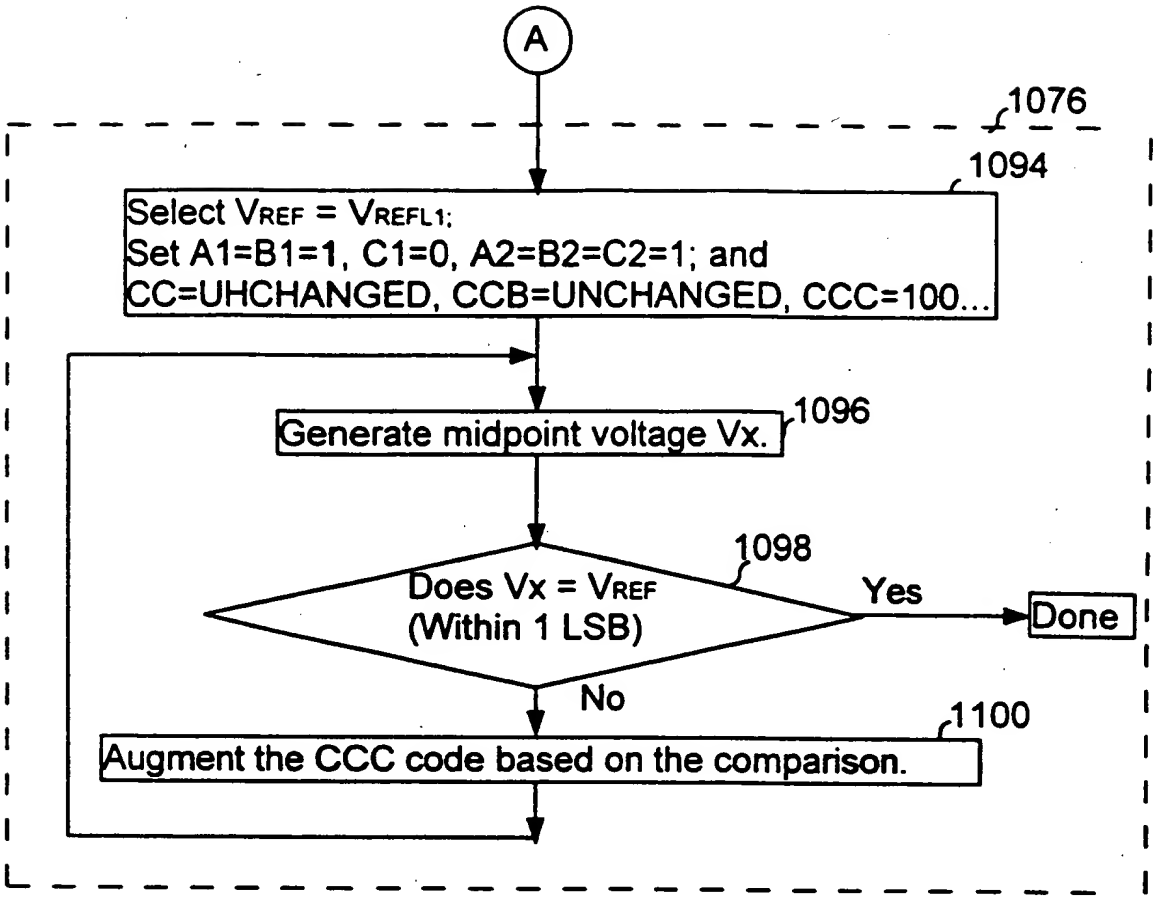
FIG. 10



Method for Calibrating the GDS Compensated Output Driver with Current Control

A

FIG. 11A



Method for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 11B

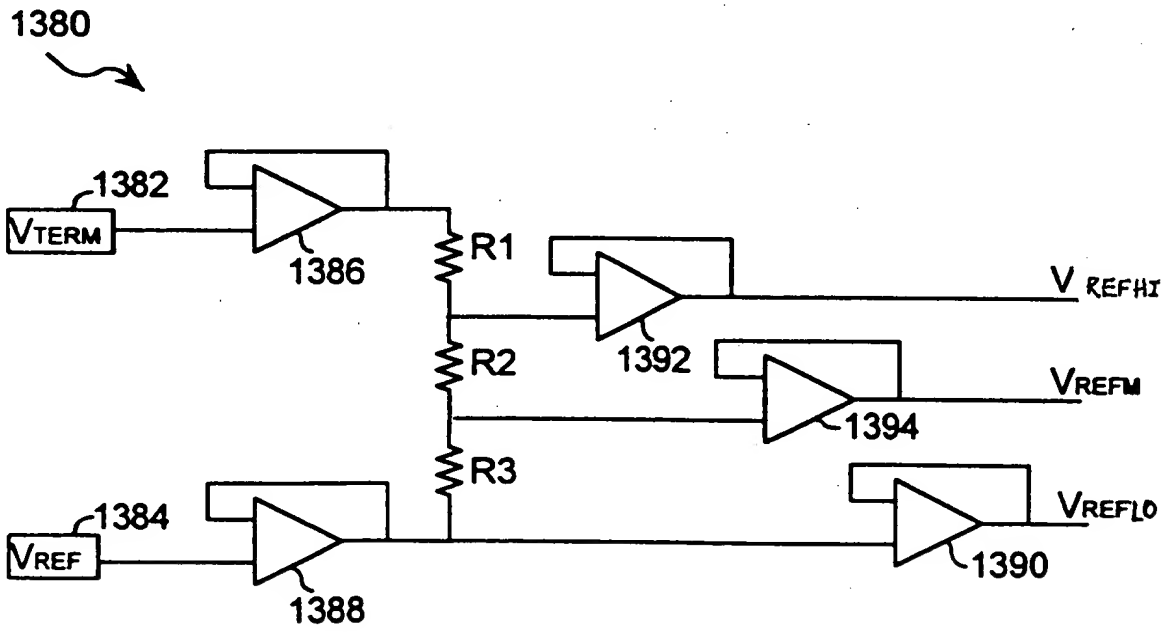

1380
1382
VTERM
1386
R1
R2
R3
1392
V REFHI
1394
VREFM
1384
VREF
1388
1390
VREFLO

FIG. 12

FIG 13A

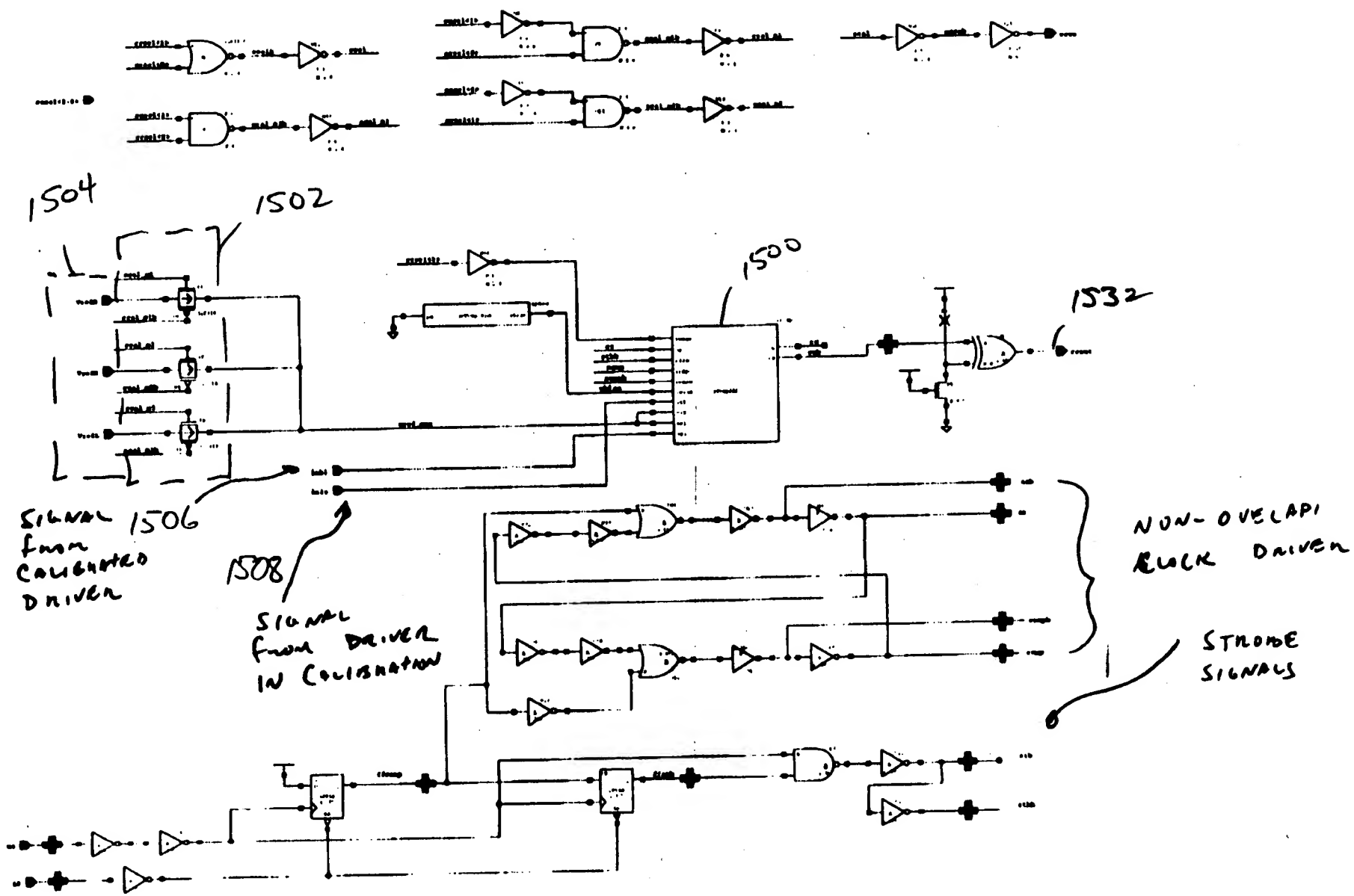
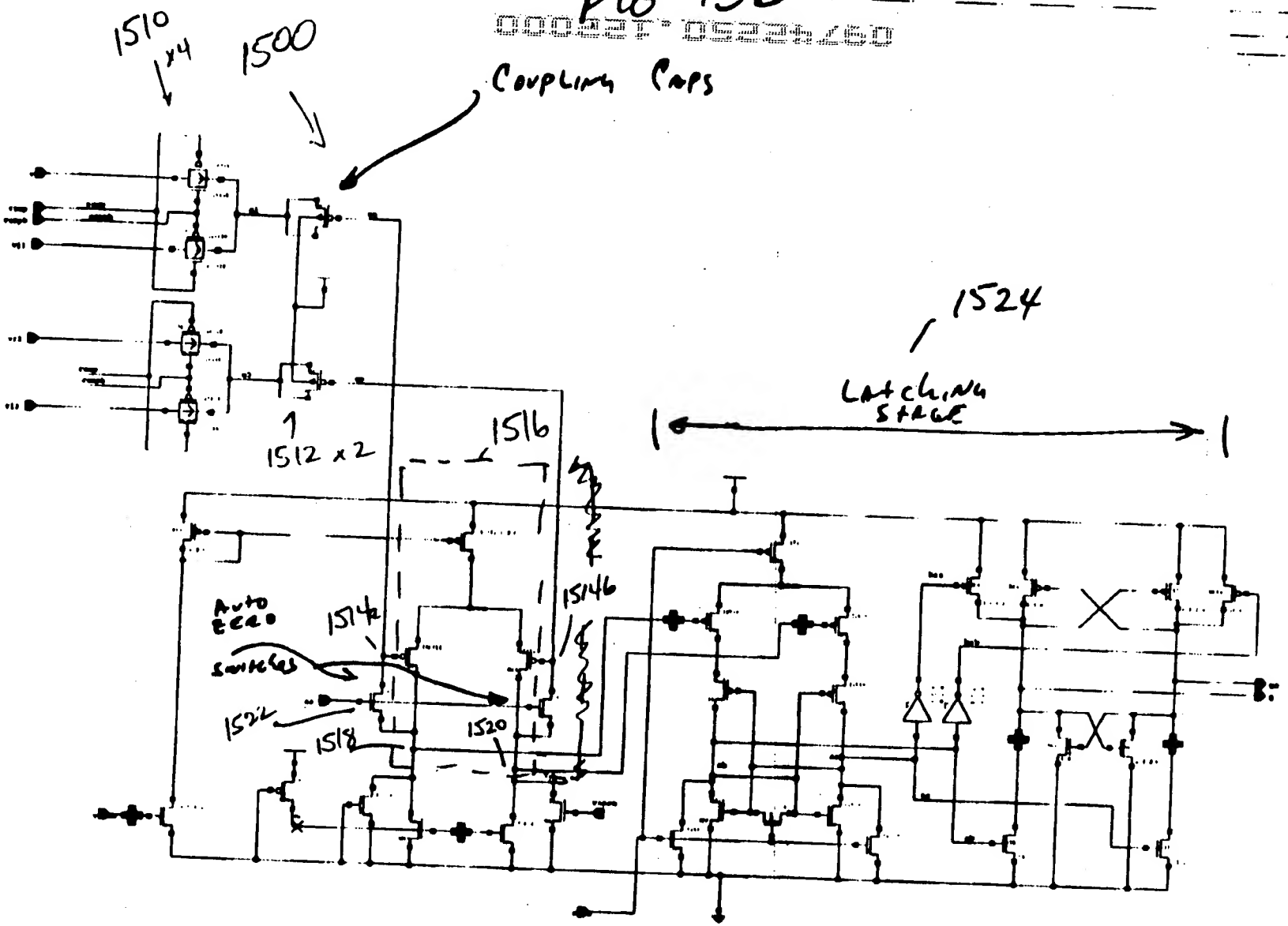

1504
1502
1500
1532
SIGNAL FROM CALIBRATED DRIVER
1506
1508
SIGNAL FROM DRIVER IN CALIBRATION
NON-OVERLAPI
CLOCK DRIVER
STROBE SIGNALS

Fig 13B


1510
x4
1500
Coupling Caps
1524
Latching Stage
1516
1512 x2
1514
1514b
Auto Eq.
switches
1512
1518
1520

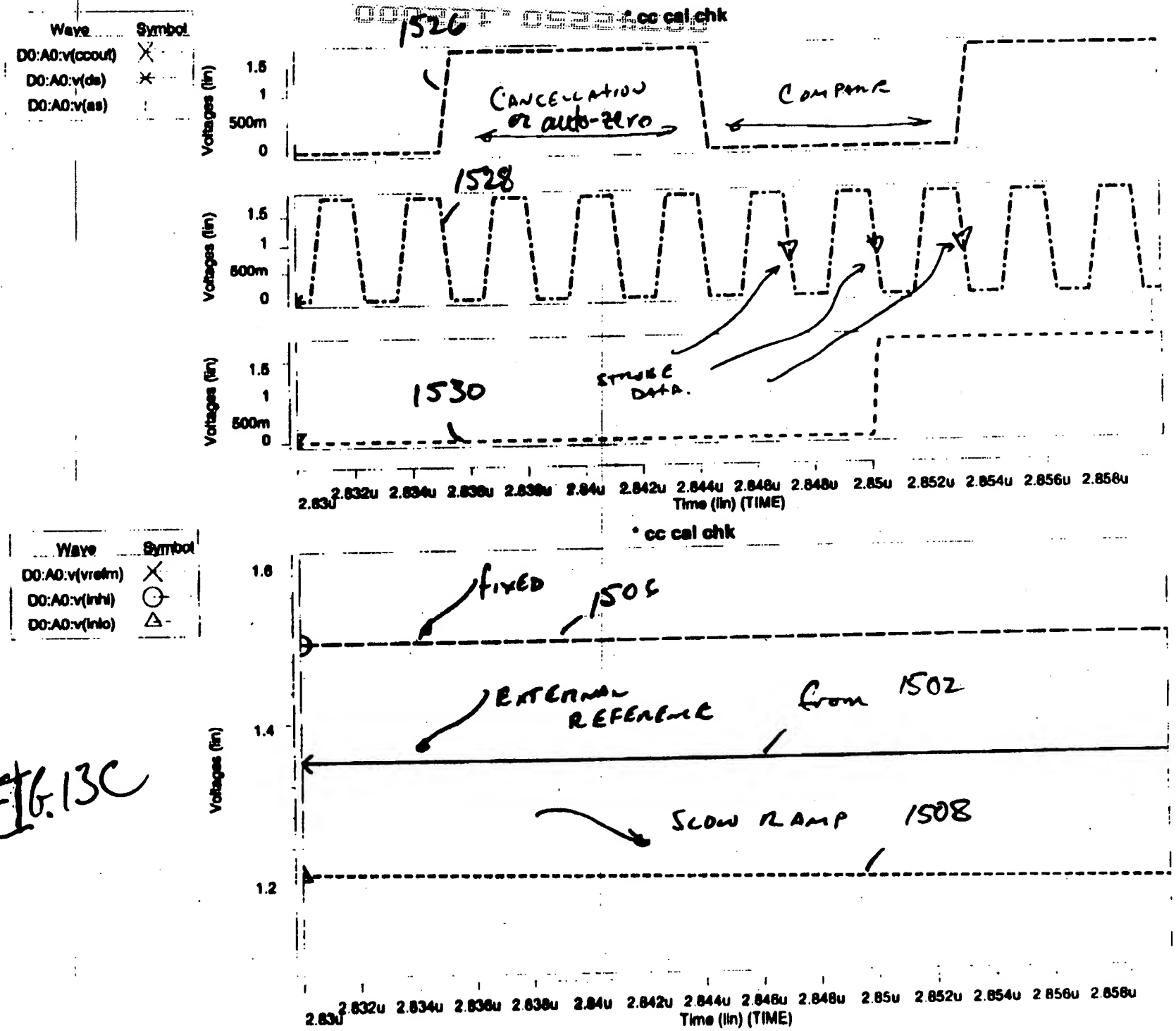
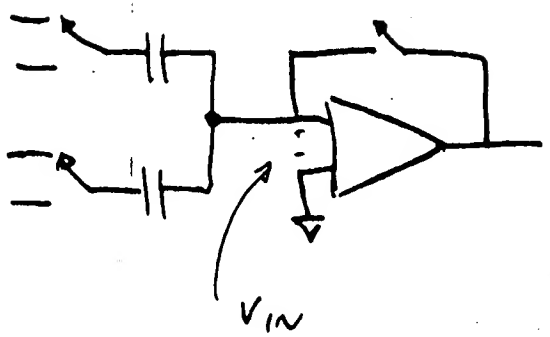

Wave
Symbol
D0:A0:v(ccout)
D0:A0:v(ds)
D0:A0:v(as)
* cc cal chk
1526
CANCELLATION OR auto-zero
COMPARE
1528
1530
STROBE DATA.
Voltages (lin)
1.5
1
500m
0
2.83u
2.832u
2.834u
2.836u
2.838u
2.84u
2.842u
2.844u
2.846u
2.848u
2.85u
2.852u
2.854u
2.856u
2.858u
Time (lin) (TIME)
Wave
Symbol
D0:A0:v(vrefm)
D0:A0:v(inhi)
D0:A0:v(inlo)
* cc cal chk
1.6
1.4
1.2
FIXED
1506
EXTERNAL REFERENCE
From 1502
SLOW RAMP
1508

FIG. 13C

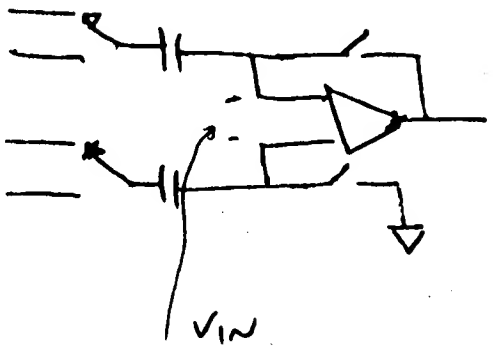
Alternate Embodiments of Differential Comparators

FIG. 13D

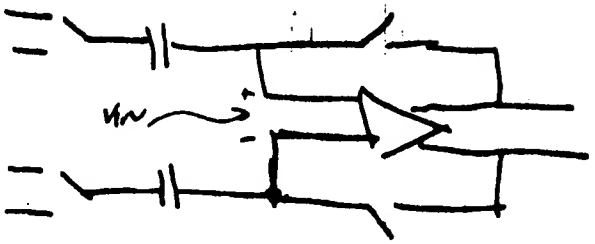


$V_{out} = A \cdot V_{IN}$

DIFFERENTIAL IN SINGLE ENDED OUT



$V_{out} = A_v$



$+ \; V_{out} = A \cdot V_{IN}$

Fig. 13E

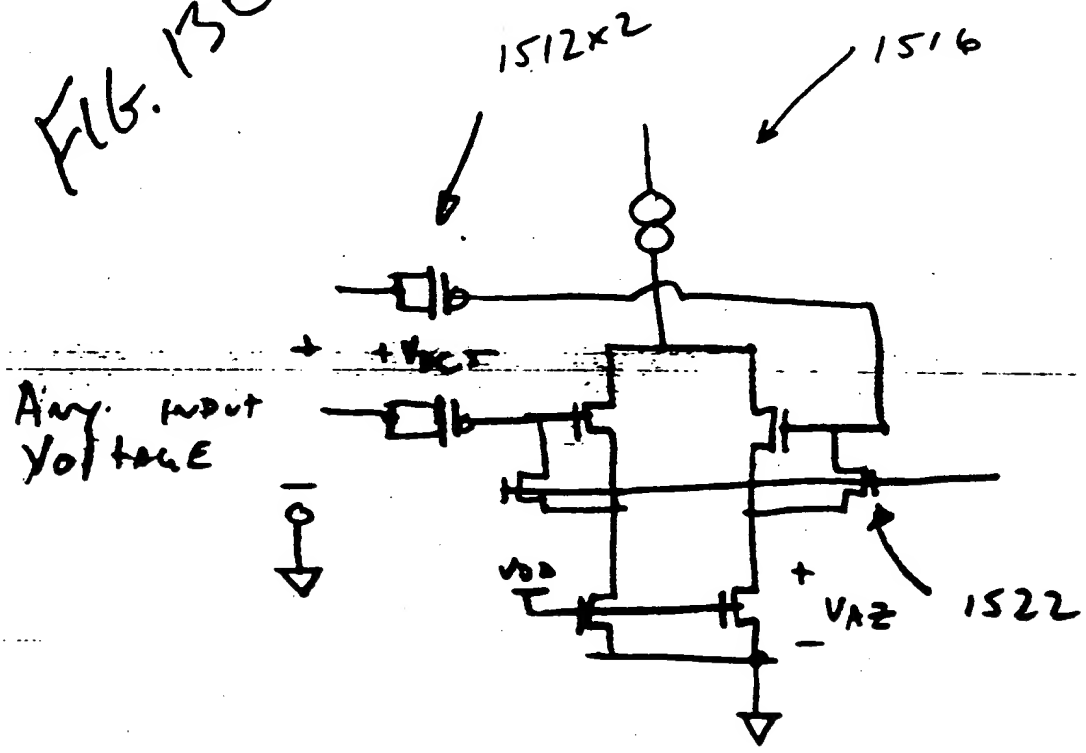


FIG 14A

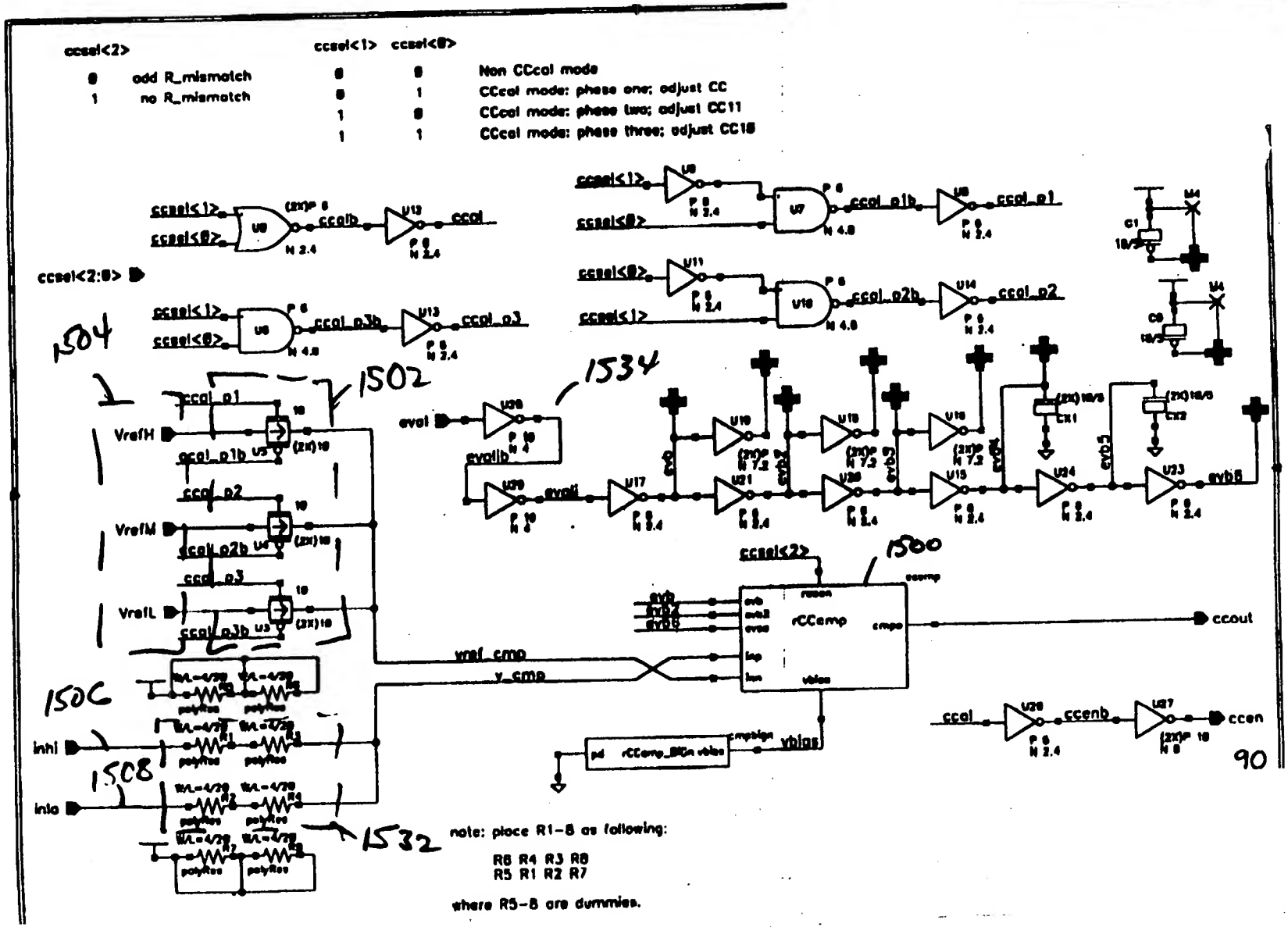

ccsel<2>
ccsel<1>
ccsel<0>
0 odd R_mismatch
1 no R_mismatch
0 0 Non CCcal mode
0 1 CCcal mode: phase one; adjust CC
1 0 CCcal mode: phase two; adjust CC11
1 1 CCcal mode: phase three; adjust CC18
ccsel<2:0>
1504
1502
1534
1500
1506
1508
1532
VrefH
VrefM
VrefL
inhi
inlo
vref_cmp
v_cmp
rCCcmp
ccout
ccen
ccal
ccenb
note: place R1-8 as following:
R6 R4 R3 R8
R5 R1 R2 R7
where R5-8 are dummies.
90

FIG 14B

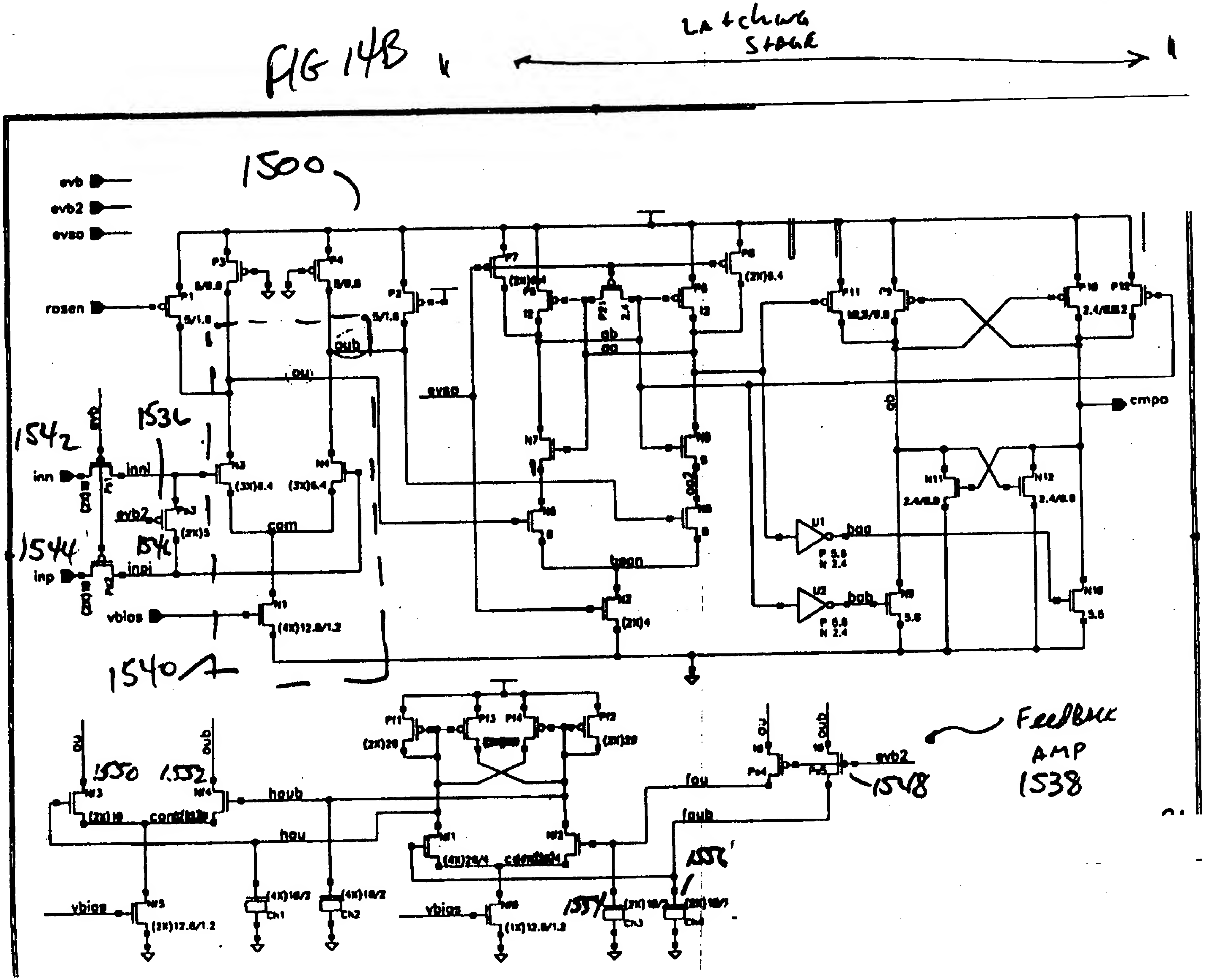

Latching stage
1500
evb
evb2
evsa
rosen
inn
inp
vbias
innl
inpl
com
ou
oub
qb
qa
cmpo
baa
bab
bqan
1536
1542
1544
1546
1540
1550
1552
1554
1556
1548
houb
hou
fou
foub
Feedback AMP 1538

Fig 14C

mismatch w/ os cancellation

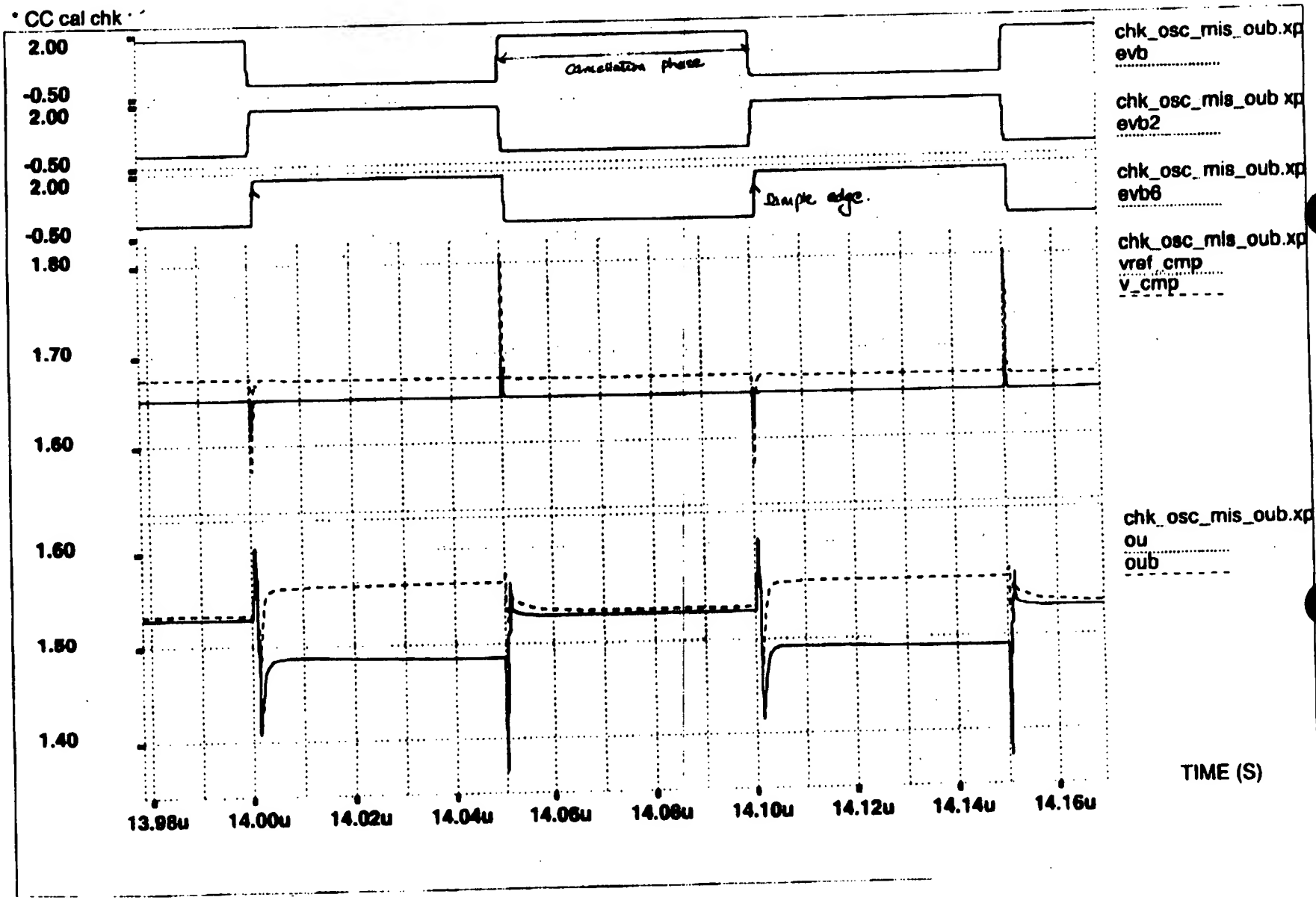


FIG 14D

w/ OS cancel

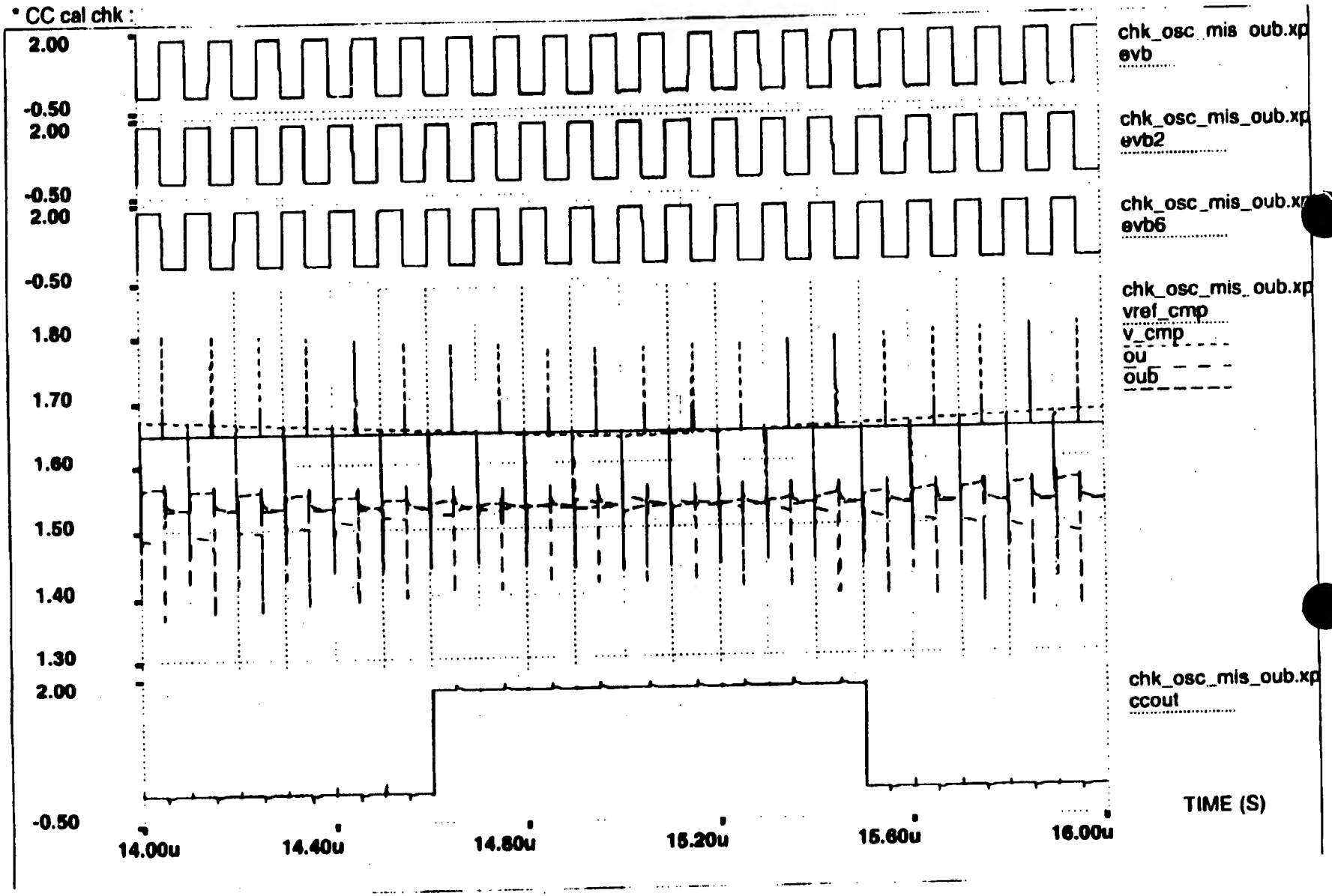
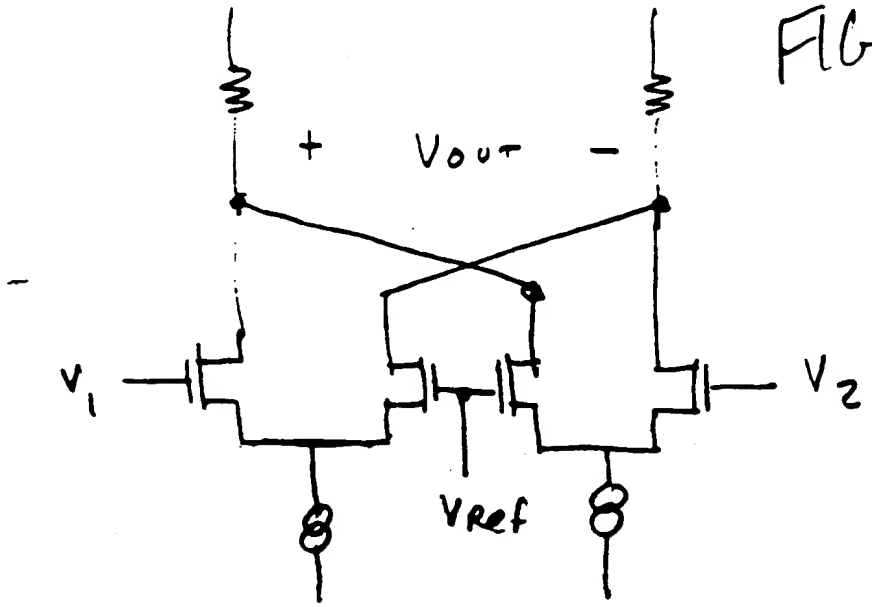
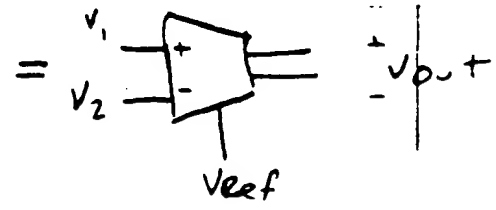


FIG. 15A





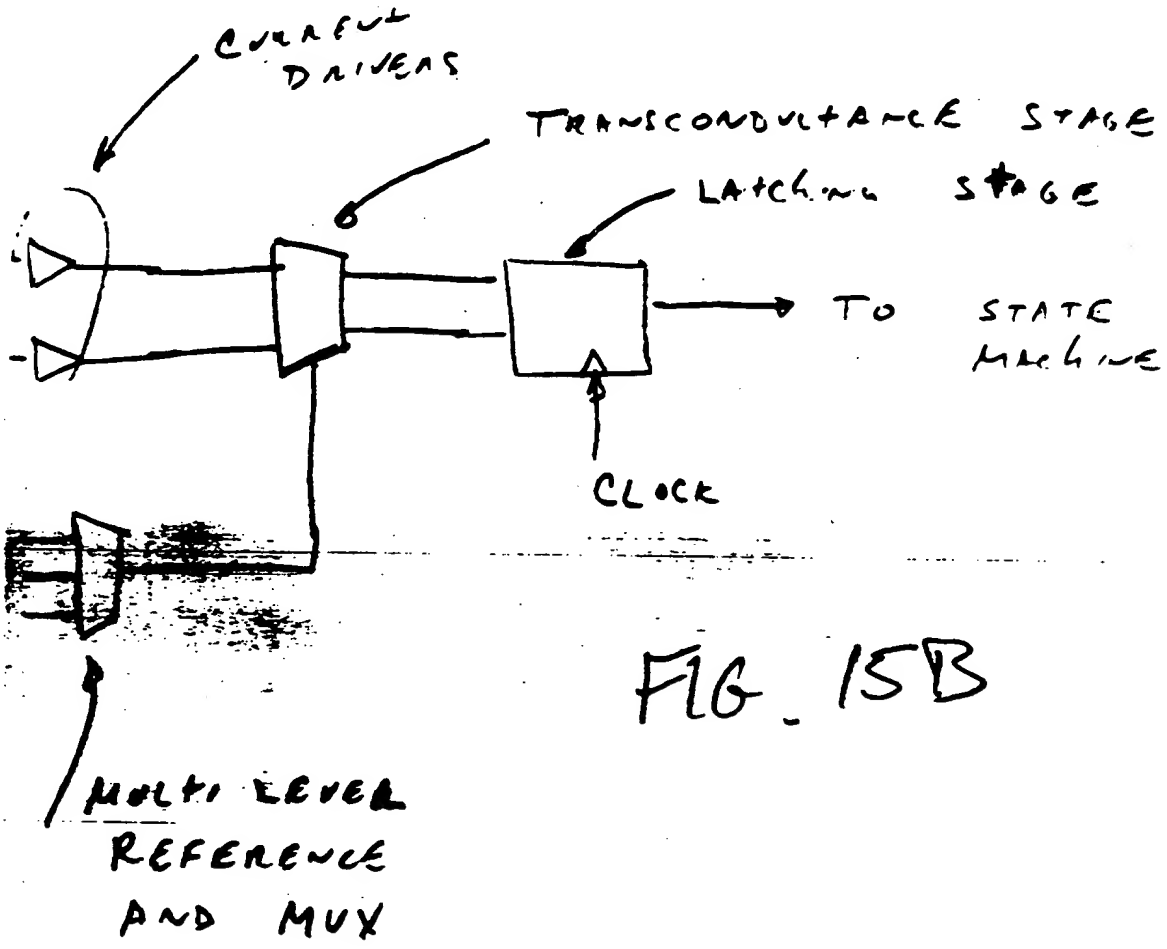

CURRENT DRIVERS
TRANSCONDUCTANCE STAGE
LATCHING STAGE
TO STATE MACHINE
CLOCK
MULTI LEVEL REFERENCE AND MUX

FIG. 15B

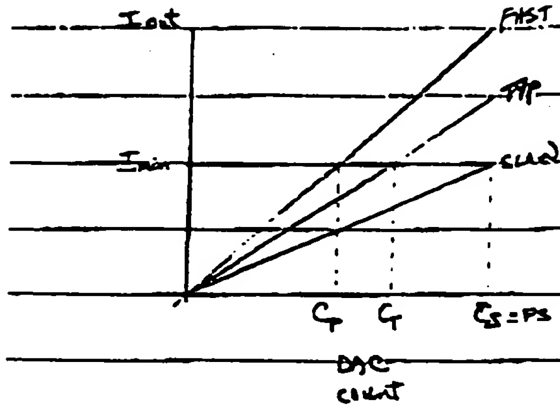


FIG. 16

Output driver block diagram:

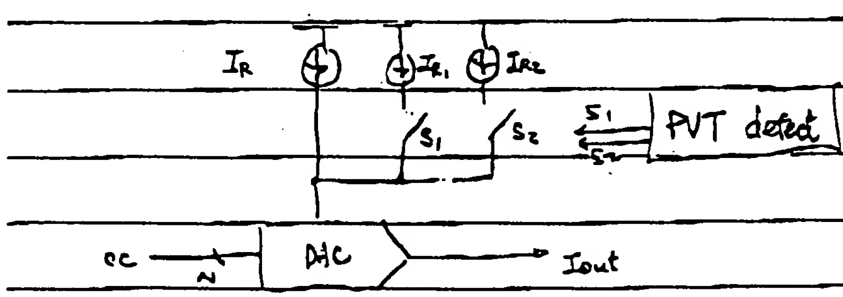
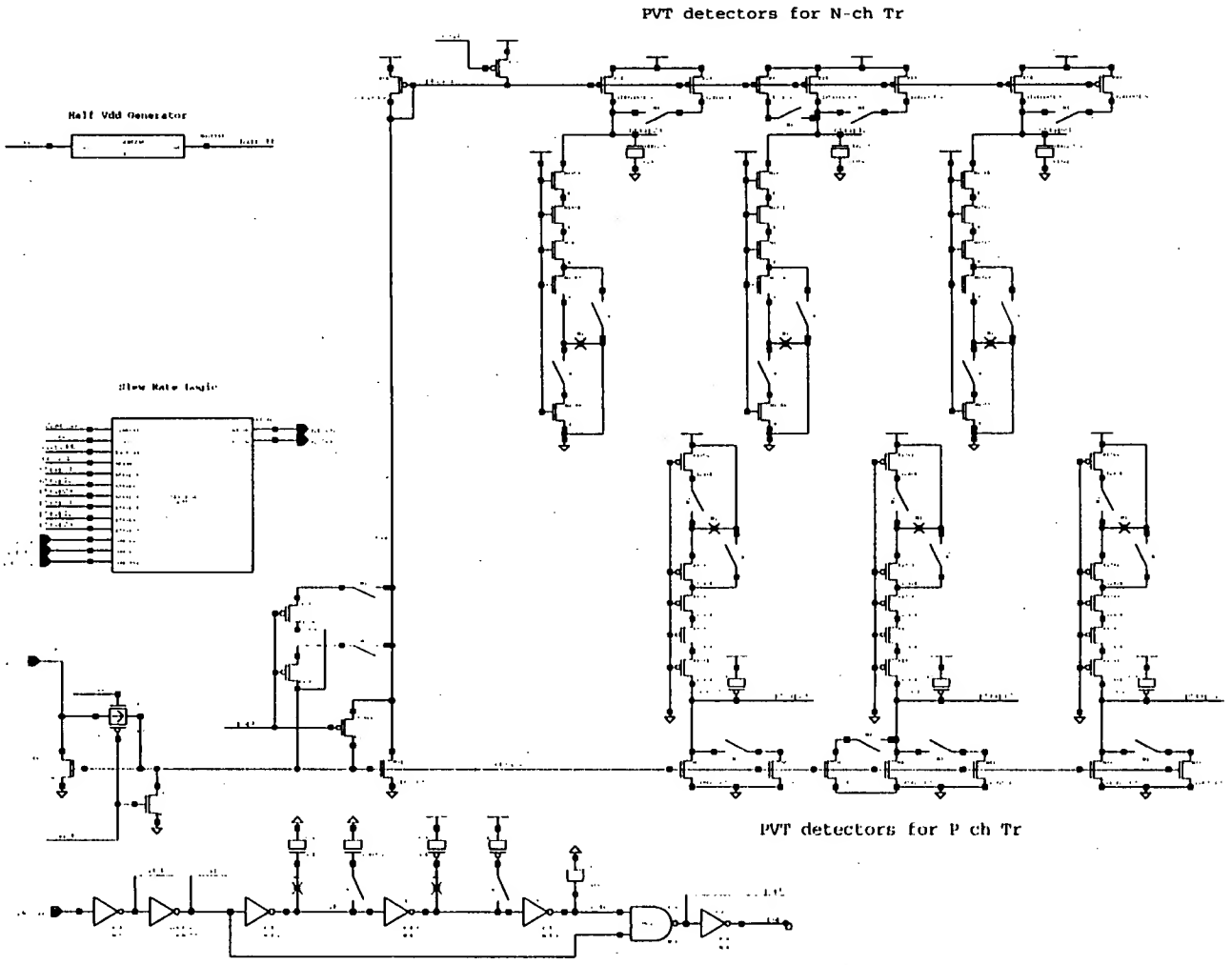


FIG. 17

FIG. 18


PVT detectors for N-ch Tr
Half Vdd Generator
Slew Rate Logic
PVT detectors for P ch Tr

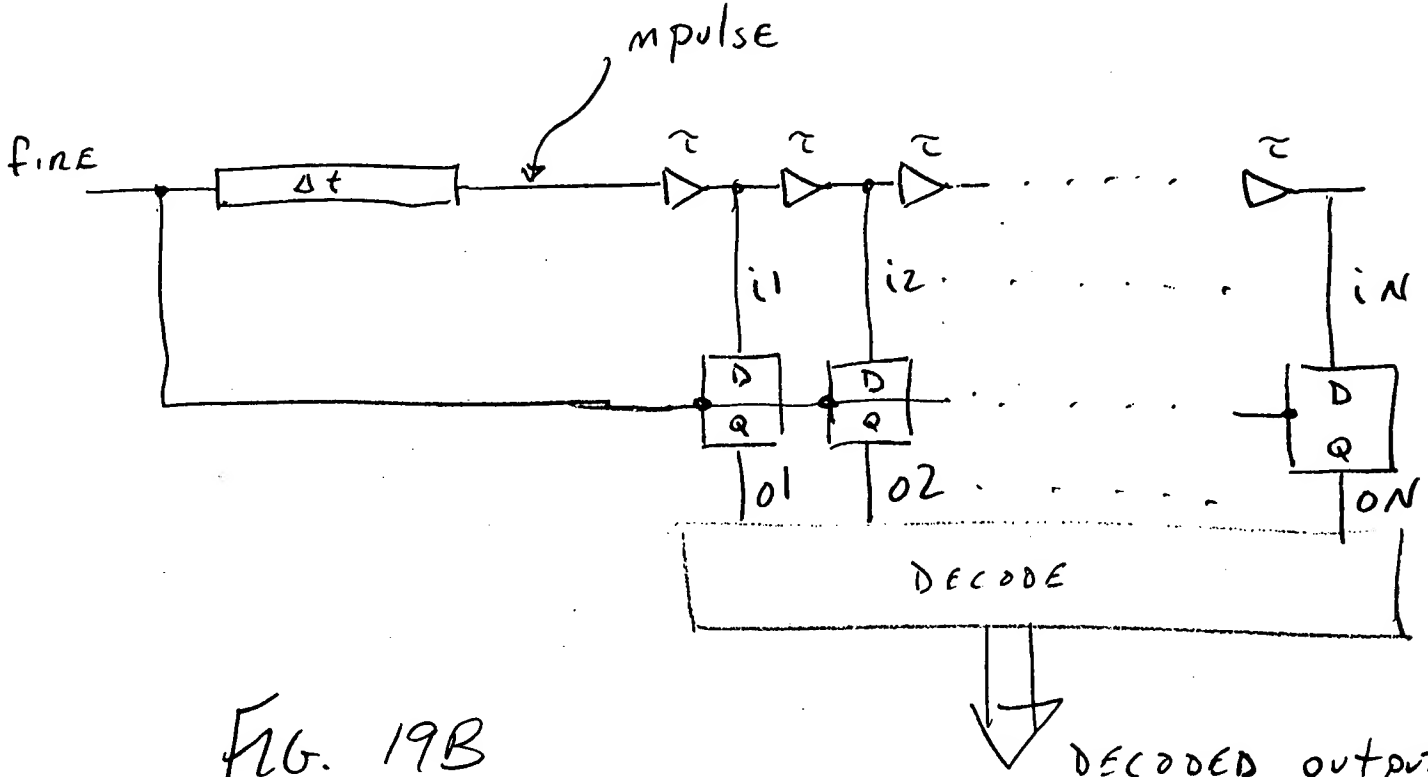


FIG. 19A

FIG. 19B

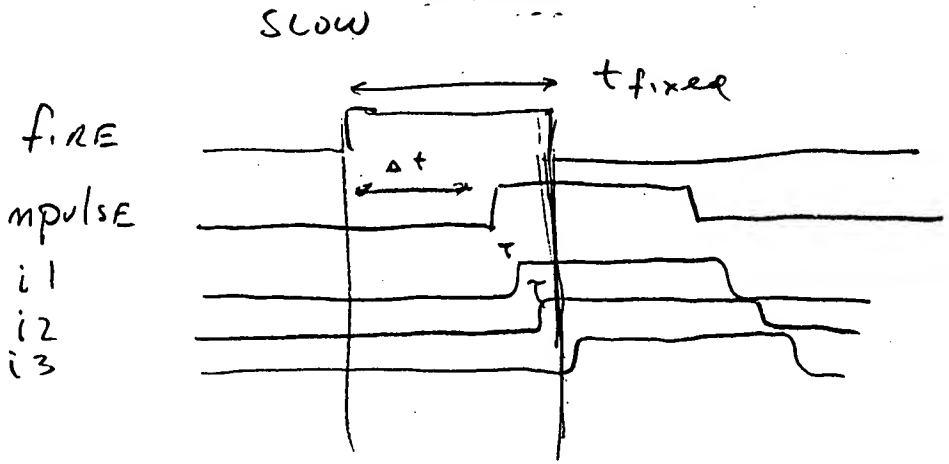


FIG 19C

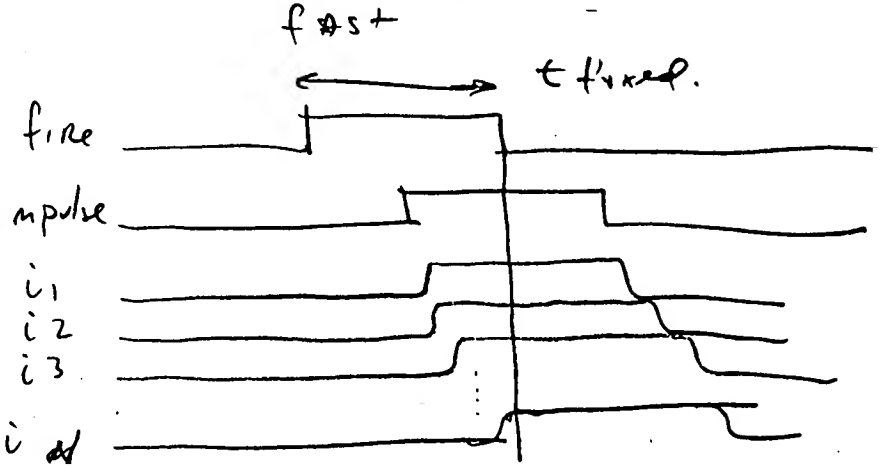
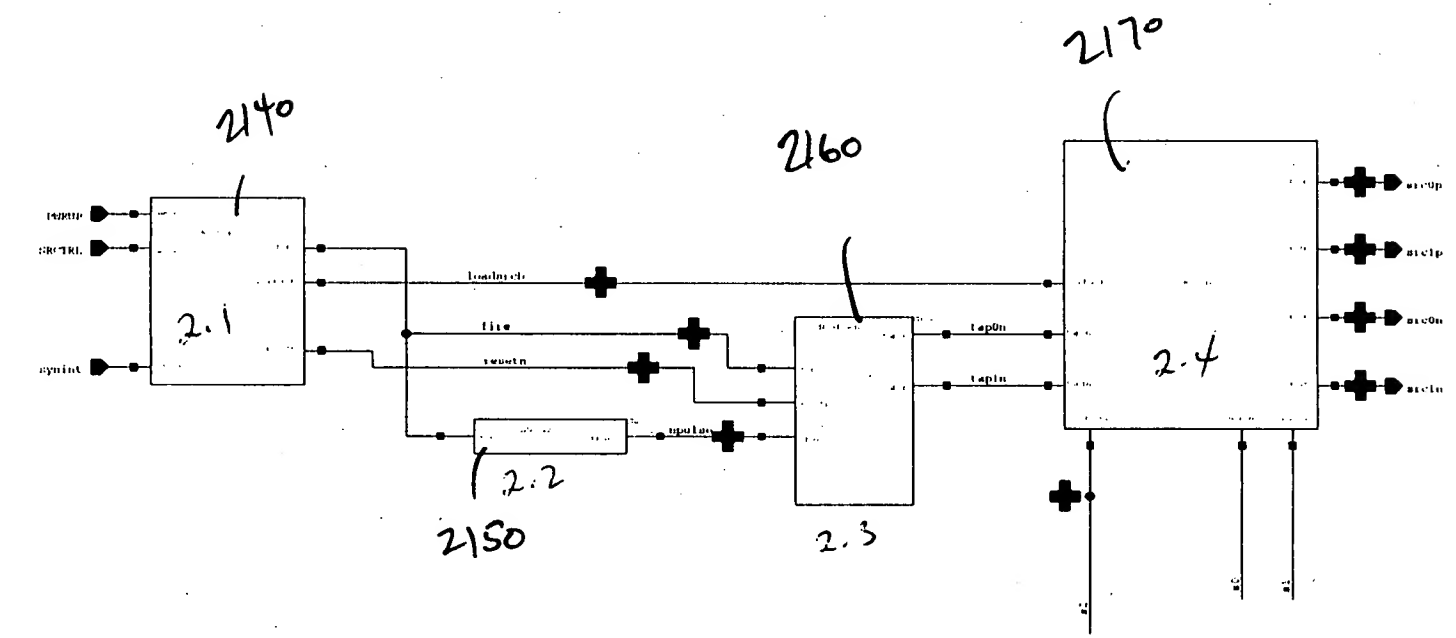


FIG 20A



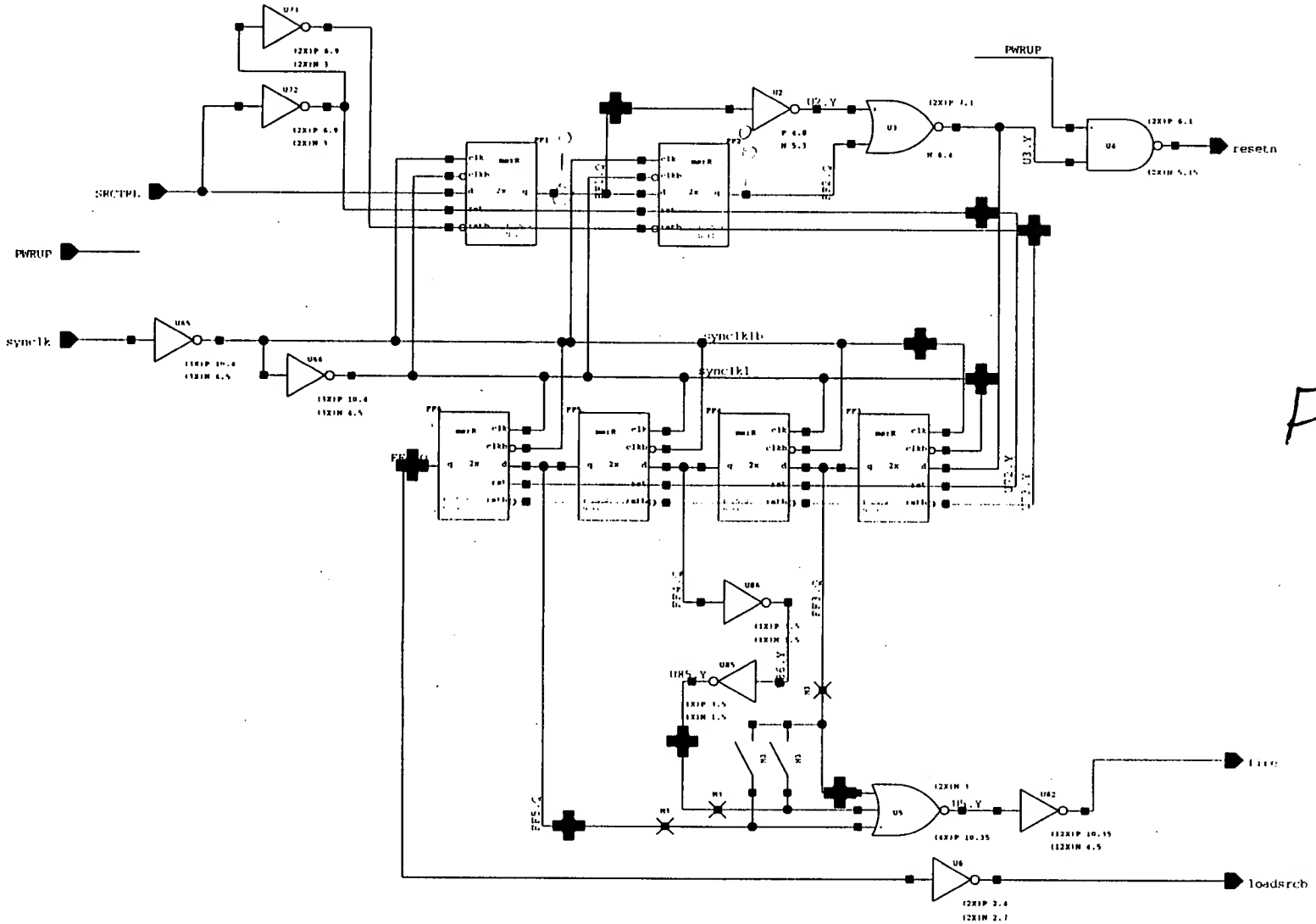

PWRUP
resetn
SRCTPL
PWRUP
sync1k
sync1k1b
sync1k1
loadsrch

FIG 20B

FIG 20C

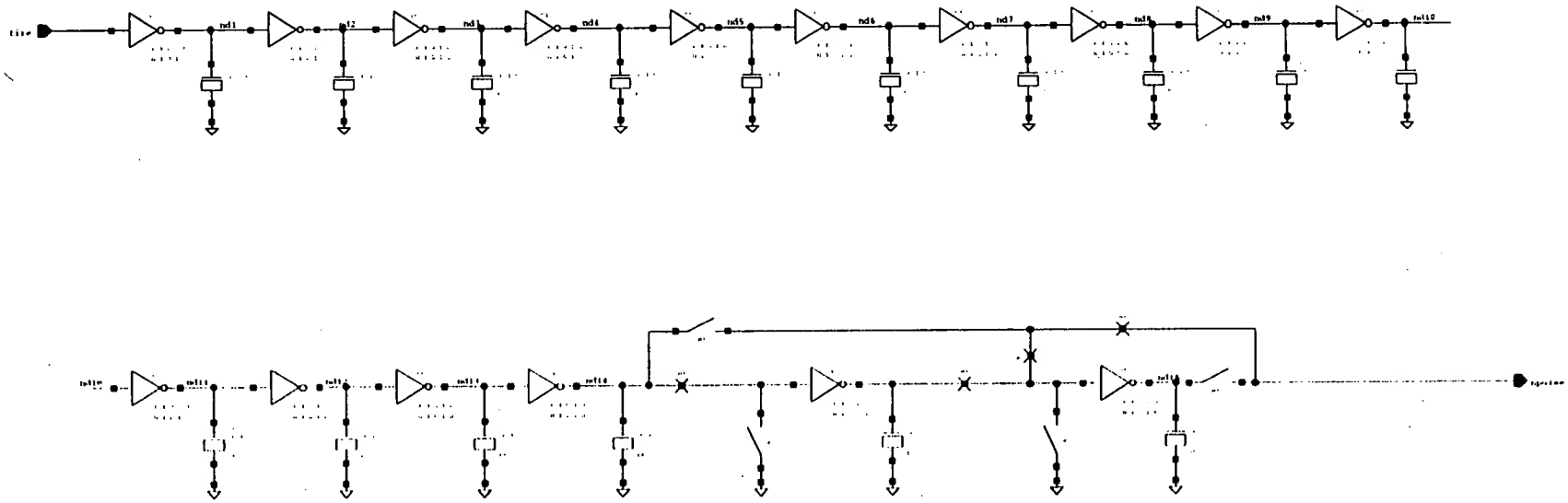


FIG. 20D

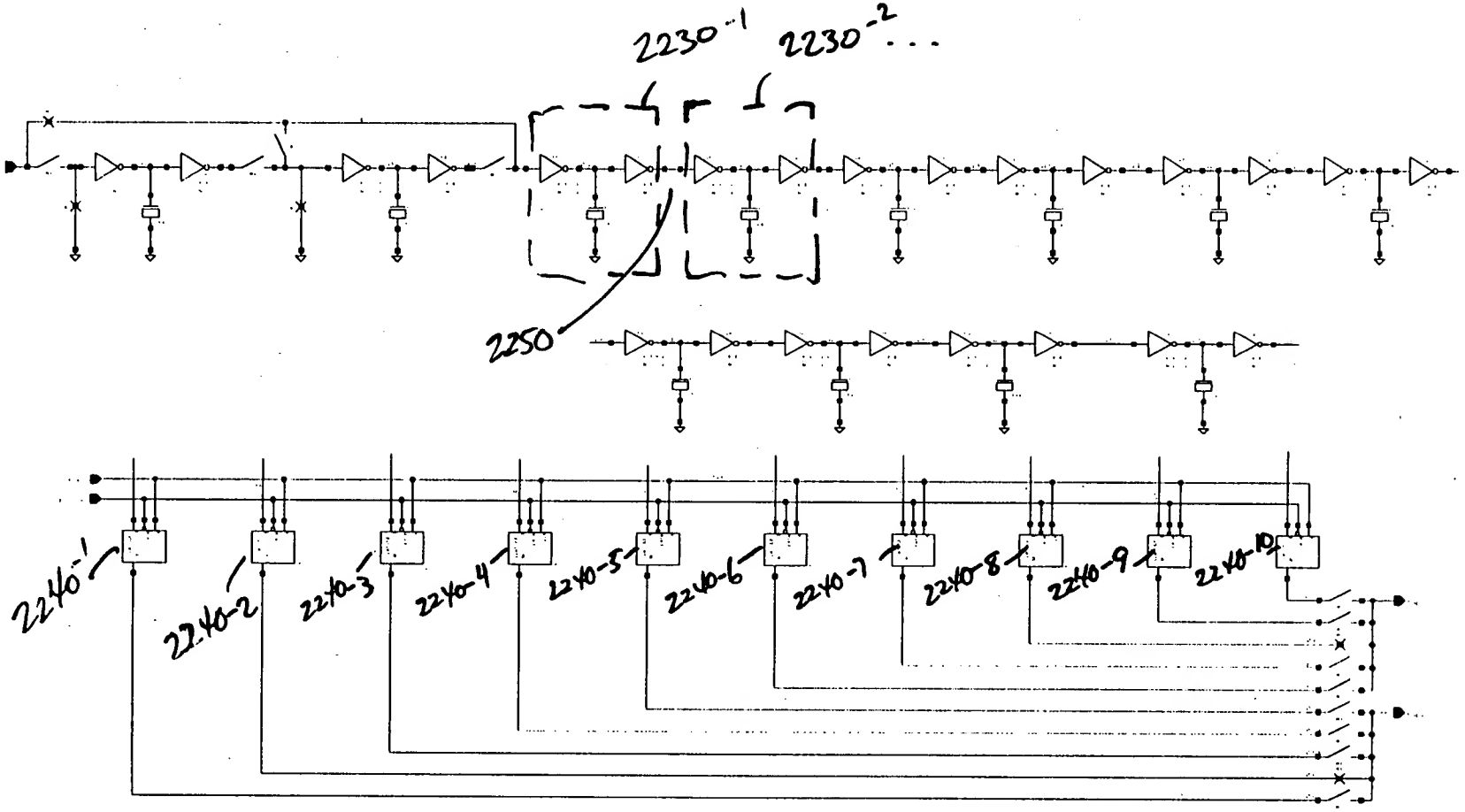
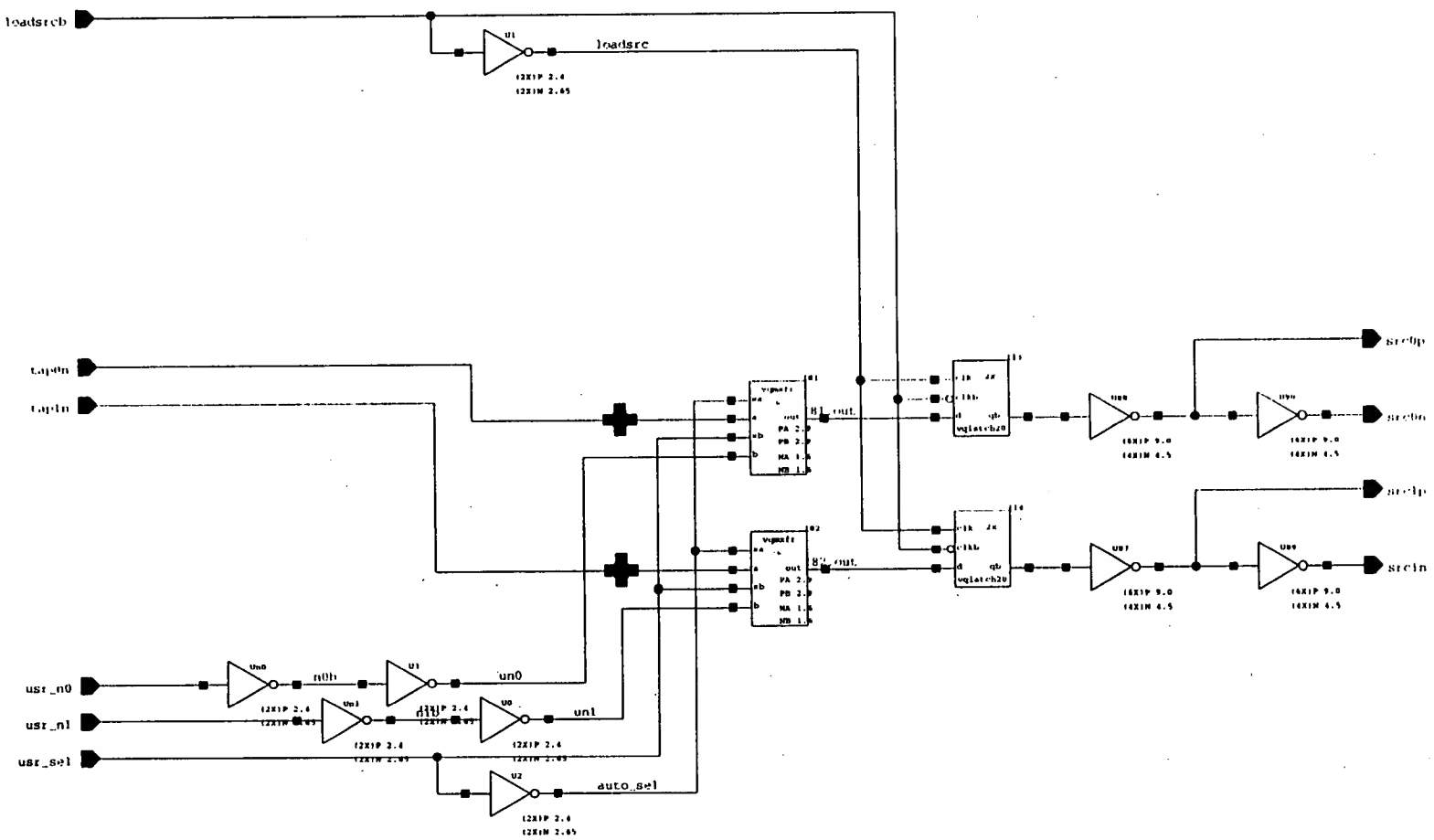

2230-1
2230-2
2250
2240-1
2240-2
2240-3
2240-4
2240-5
2240-6
2240-7
2240-8
2240-9
2240-10

FIG 20E


loadsrcb
loadsrc
tapdn
tapin
usr_n0
usr_n1
usr_sel
n0b
un0
un1
auto_sel
srcdp
srcdn
srcip
srcin

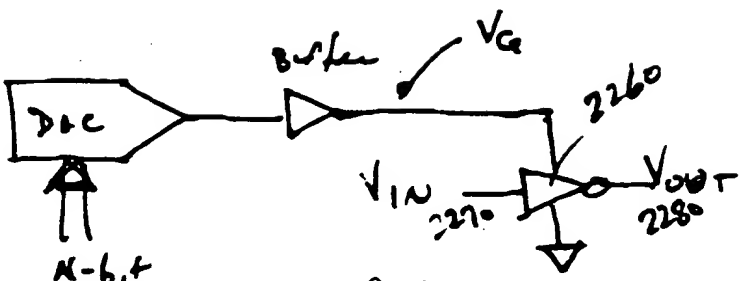


FIG 21A

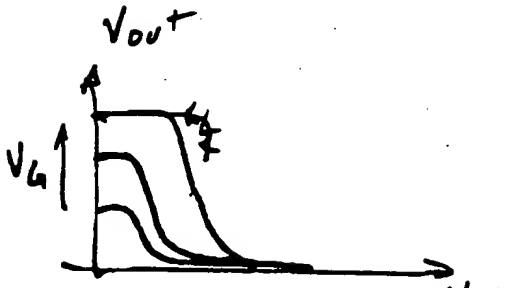


FIG 21B

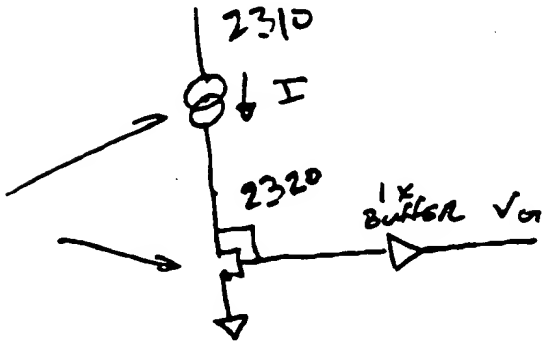


FIG 22

Alternate Embodiment of Vgate DAC

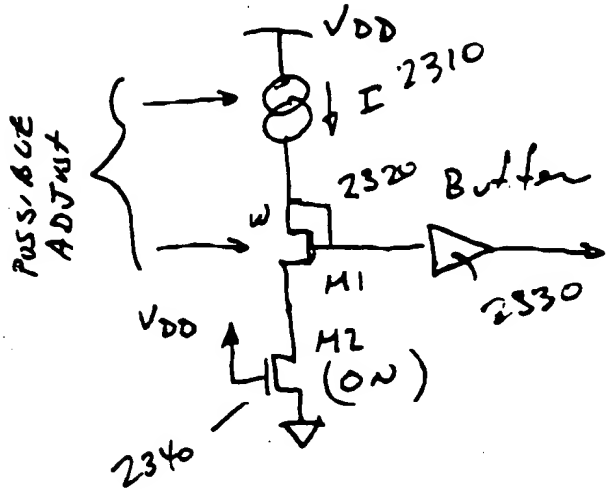


Fig. 23

M1, M2 scaled to match actual output driver.

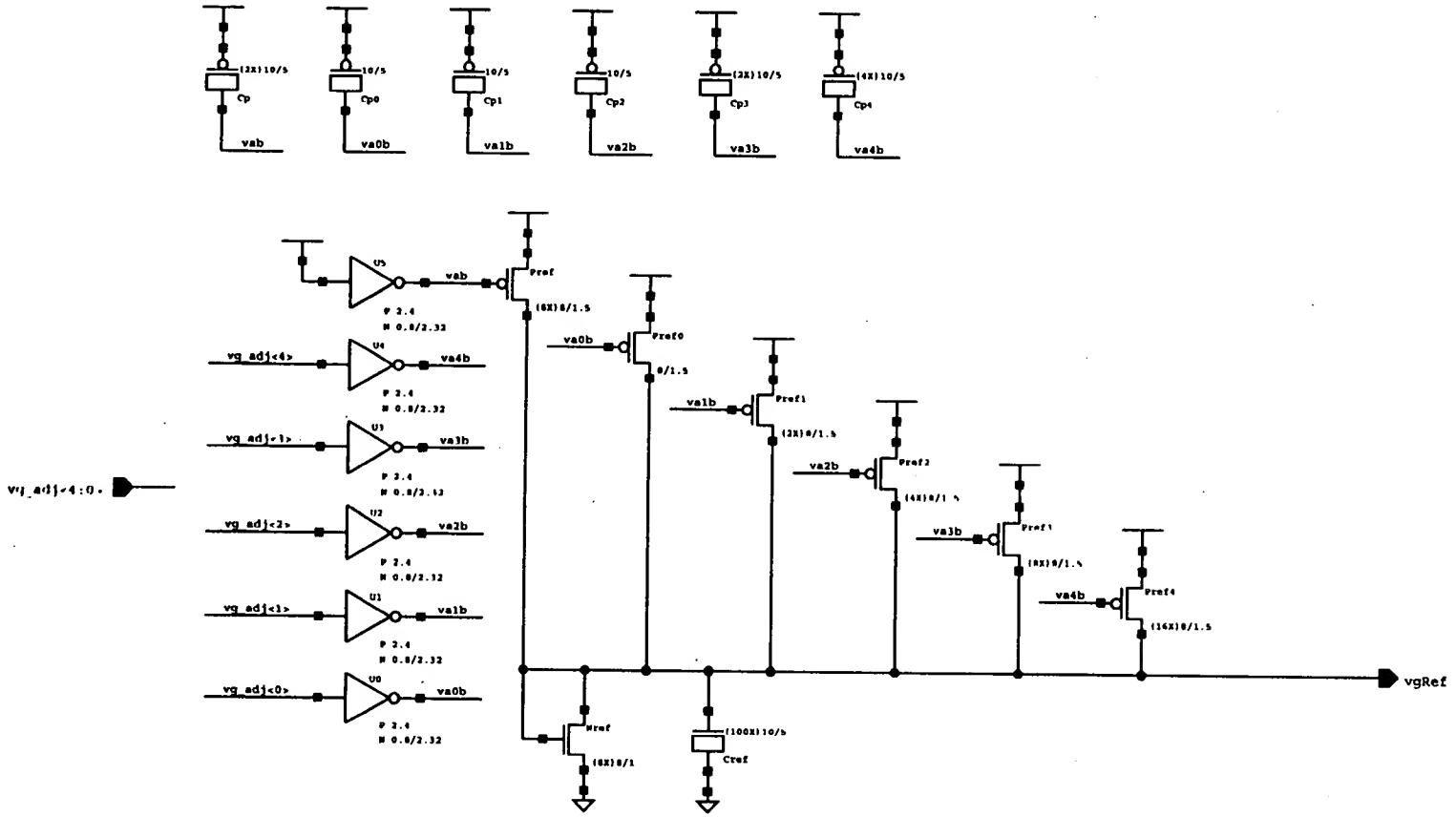


Fig. 24A

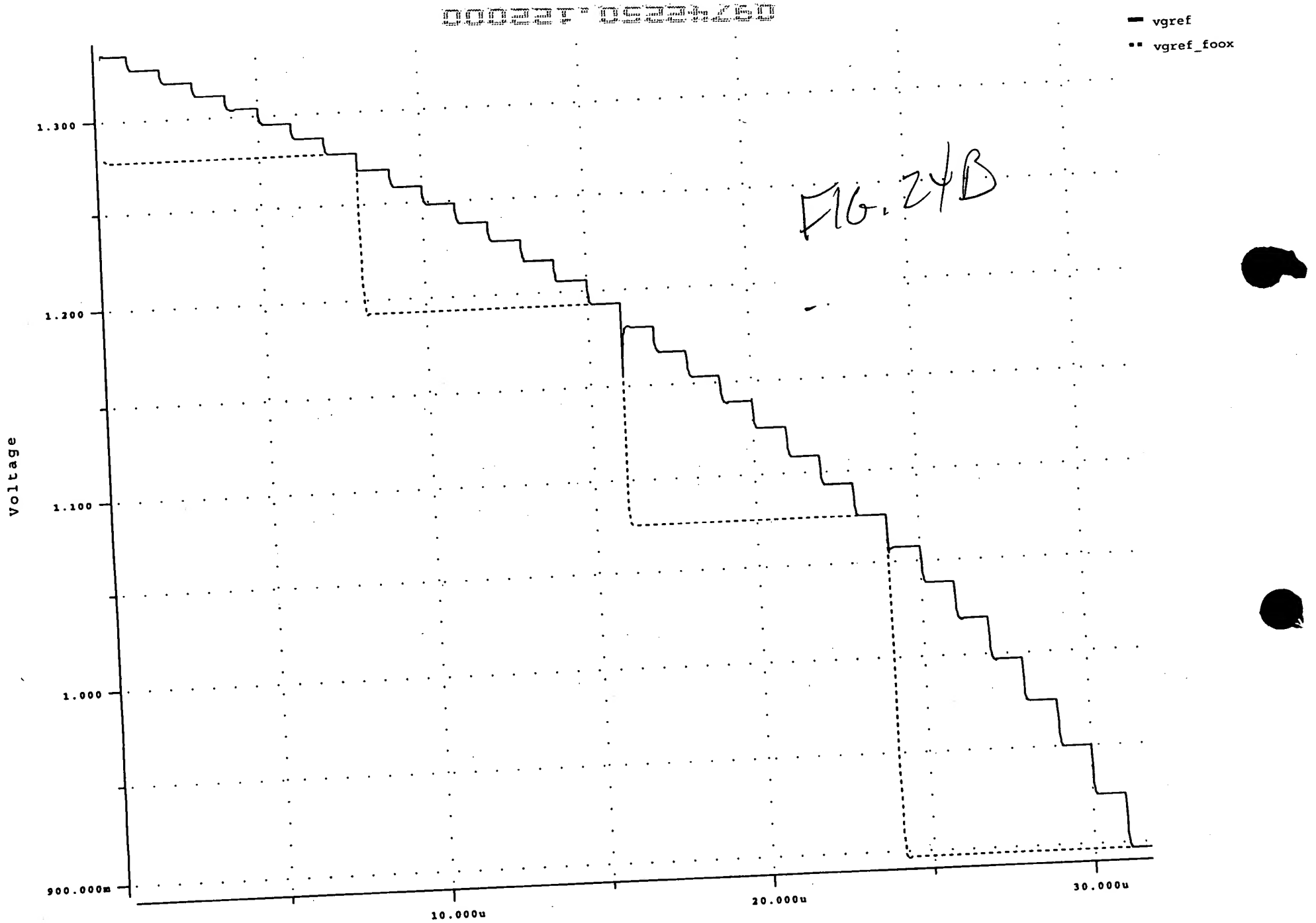

vgref
vgref_foox
1.300
1.200
1.100
1.000
900.000m
Voltage
10.000u
20.000u
30.000u

FIG. 24B